Hybrid Graphene Nanoribbon-CMOS Tunneling Volatile Memory Fabric

Santosh Khasanvis, K. M. Masum Habib, Mostafizur Rahman, Pritish Narayanan,
Roger K. Lake and Csaba Andras Moritz
khasanvis@ecs.umass.edu, andras@ecs.umass.edu

***Abstract*— Graphene exhibits extraordinary electrical properties and is therefore often envisioned to be the candidate material for post-silicon era as Silicon technology approaches fundamental scaling limits. Various Graphene based electronic devices and interconnects have been proposed in the past. In this paper, we explore the possibility of a hybrid fabric between CMOS and Graphene by implementing a novel Graphene Nanoribbon crossbar (xGNR) based volatile Tunneling RAM (GNT RAM) and integrating it with the 3D CMOS stack and layout. Detailed evaluation of GNT RAM circuits proposed show that they have considerable advantages in terms of power, area and write performance over 16nm CMOS SRAM. This work opens up other possibilities including multi-state memory fabrics and even an all-graphene fabric can be envisioned on the long term.**

Keywords- Graphene Nanoribbons; NDR; Volatile Memory; Hybrid Integration.

I. INTRODUCTION

Silicon CMOS technology, which has been the foundation of digital integrated circuits, has experienced an exponential growth during the past fifty years mainly due to its unique scaling properties. However, CMOS scaling is approaching fundamental limits due to various factors such as increased power density, leakage currents and production costs with diminishing performance returns. Faster computing systems need access to large amounts of on-chip memory and Silicon technology scaling limits create bottlenecks in realizing high density memory. Given the technological and financial limitations, there are increasing incentives to explore new avenues to implement the required function. While some of the directions look at new types of devices (such as cross-nanowire transistors [1], [2], [3]), others explore novel physical phenomena (using electron spin [4] instead of charge) and alternative materials such as carbon, to build electronic devices and circuits.

Graphene, a 2-dimensional (2D) monolayer of carbon atoms arranged in honeycomb structure, has exotic electronic and mechanical properties featuring the Dirac fermion [5] with high mobility [6] and a long coherence length. Due to these properties and extreme scalability down to the atomic level [7], Graphene is envisioned to be the candidate material for post-Silicon era. However, a lack of bandgap in 2D graphene [8] reduces its utility for conventional electronic device applications. One way of introducing a bandgap is to confine electrons by patterning a 2D graphene sheet into a narrow (<10nm) ribbon, better known as a graphene nanoribbon (GNR) [9], [10]. Another way to modify the band structure of graphene is to stack two monolayers to form a bilayer which has a semiconducting band structure with zero bandgap [11]. This bandgap can be additionally tuned by creating a potential difference between the two layers [12], [13].

The performance of field effect transistors (FETs) using bilayer graphene as the channel material was recently studied [14]. It was shown that such a FET had a poor on-off current ratio, I_{on}/I_{off}, due to strong band-to-band tunneling. However, a tunnel FET using bilayer graphene showed promising performance [15]. Other proposed devices include a nanoelectromechanical FET based on interlayer distance modulation [16], [17], a FET utilizing a bilayer exciton condensate [18] and GNR junction diodes featuring negative differential resistance (NDR) based on chemical [19] and field effect [20] doping.

Recently, electronic transport through a bilayer GNR structure has been studied numerically by [21]. The geometry consists of two GNRs placed on top of each other in AA or AB sequence with an external bias applied to one with respect to the other. It has been shown that NDR occurs in such structure. Reference [22] considers a more realistic geometry consisting of two GNRs placed on top of each other at right angles like a crossbar. Calculations, based on ab-initio density functional theory (DFT) coupled with the non-equilibrium Green's function (NEGF) formalism, reveal that NDR also occurs in the model GNR crossbar (xGNR).

In this paper, we propose a hybrid 3D integration between CMOS and Graphene to implement a novel Graphene NanoRibbon crossbar based Tunneling volatile Random Access Memory (GNT RAM) utilizing a Bi-Layer Graphene NanoRibbon crossbar device (xGNR) [22]. Such cross-technology integration for volatile memory has not been explored yet to the best of our knowledge. We evaluate the GNT RAM in terms of power, performance and area and show a comparison with 16nm CMOS SRAM. Our analysis shows that GNT RAM has considerable advantages over 16nm CMOS SRAM in terms of power dissipation, area and write performance. As progress is made in Graphene technology, substituting CMOS components with graphene devices to realize all-graphene volatile memory fabrics can do further optimization.

Santosh Khasanvis, Mostafizur Rahman, Pritish Narayanan and Csaba Andras Moritz are with University of Massachusetts at Amherst, Amherst, MA 01003 USA.

K. M. Masum Habib and Roger K. Lake are with University of California Riverside, Riverside, CA 92521-0204 USA.

The rest of the paper is organized as follows. Section II introduces Bi-Layer Graphene Nanoribbon crossbar device (xGNR) which exhibits Negative Differential resistance (NDR), and discusses its application as a latch. Section III contains details about the proposed GNT RAM and Section IV describes 3D hybrid integration between CMOS and Graphene. Methodology and Simulation are discussed in Section V. Section VI presents the evaluation and comparison of GNT RAM with CMOS SRAM, followed by conclusion in Section VII.

II. BiLayer Graphene NanoRibbon Crossbar

A. xGNR NDR Device

The model xGNR structure consists of a vertical and a horizontal semi-infinite, H-passivated, armchair type GNR (AGNR) placed one on top of the other at right angles as shown in Fig. 1 [22]. The widths of the GNRs are chosen to be 14-C atomic layers ($3n + 2$) ~1.8 nm to minimize the bandgap resulting from the finite width. The bandgap of the 14-AGNR calculated from DFT code, Fireball [23], [24], is 130meV, which is in good agreement with Son *et al*. [25].

The extended regions of the vertical GNR (hGNR) and the horizontal GNR (vGNR) act as contacts. A bias is applied to the vGNR with respect to the hGNR. Each GNR is independently contacted such that hGNR is held at ground while vGNR has a bias applied to it. Independently contacting the vGNR and the hGNR maximizes the voltage drop between them. Assuming that the majority of the potential drop occurs between the two GNRs, the potential difference between the two nanoribbons is then the applied bias.

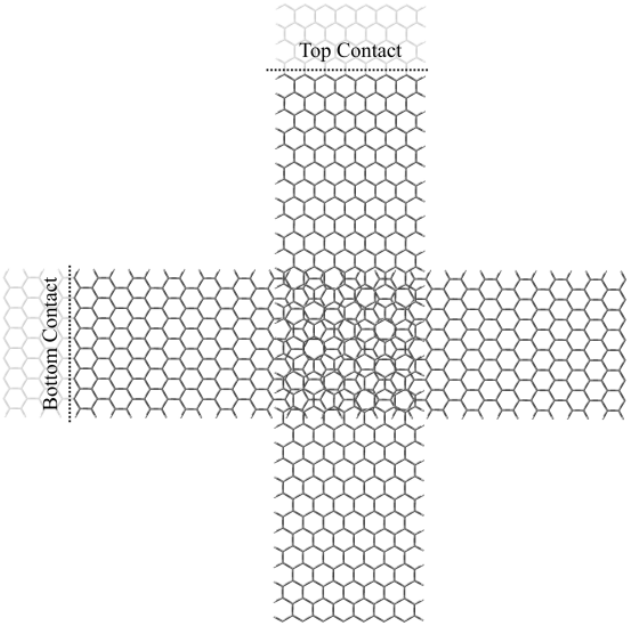

Figure 1. Atomistic geometry of the GNR crossbar. Two hydrogen passivated relaxed armchair type GNRs are placed on top of each other at a right angle with a vertical separation of 3.35 Å. The relaxation was done using Fireball. The extended parts of the GNRs are used as contacts. A bias is applied by independently contacting each GNR such that one is held at ground while the other has a potential applied to it.

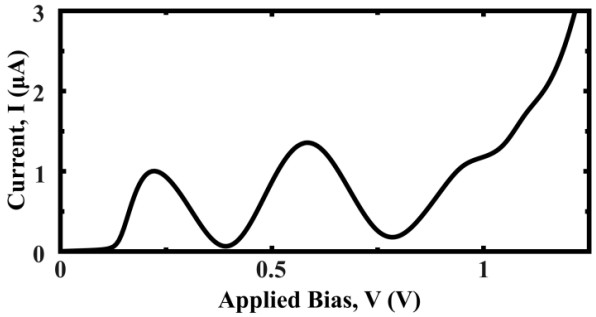

Figure 2. Simulated *I-V* characteristics of the crossbar structure exhibiting NDR. The first peak and the valley currents occur at 0.2 V and 0.4 V and the second peak and the valley currents occur at 0.6 V and 0.8 V respectively [22].

The electronic structure of the GNRs and xGNR is modeled with the quantum molecular dynamics, DFT code, Fireball, using separable, nonlocal Troullier-Martins pseudopotentials [26], the BLYP exchange correlation functional [27], [28], a self-consistent generalization of the Harris-Foulkes energy functional [29], [30] known as DOGS after the original authors [31], [32], and a minimal sp^3 Fireball basis set. The radial cutoffs of the localized pseudoatomic orbitals forming the basis are $r_c^{1s} = 4.10$ Å for hydrogen and $r_c^{2s} = 4.4$ Å and $r_c^{2p} = 4.8$ Å for carbon [33].

Fireball Hamiltonian matrix elements are used in the NEGF algorithm to calculate the surface self-energies, Green's function of the device, the spectral function, the transmission, and the current as described in [34].

The simulated *I-V* characteristics of the xGNR corresponding to Fig. 1 are shown in Fig. 2. Like bilayer GNR discussed in [21], the xGNR structure exhibits Negative Differential Resistance (NDR). However, unlike the former, the latter has two peak and two valley currents. The first peak and valley currents, 0.94 μA and 0.07 μA, occur at 0.2 V and 0.4 V respectively and the second peak and valley currents, 1.33 μA and 0.19 μA, occur at 0.6 V and 0.8 V respectively.

B. Application of xGNR Device as a latch

The bi-layer crossbar GNR device (xGNR) displays NDR characteristics which can be used in RTD-based applications [35]-[38]. We explore one possible direction where xGNR devices are used in a latch configuration in a volatile memory cell [37]. The xGNR device is represented using the symbol shown in Fig. 3a. A series stack of two xGNR devices (Fig. 3b) exploits NDR characteristics to exhibit multiple stable states A, B & C as shown in Fig. 3c. This xGNR series configuration can be used as a binary latch or multi-state latch, where the bit is stored on the common terminal (the state node) of the xGNR devices.

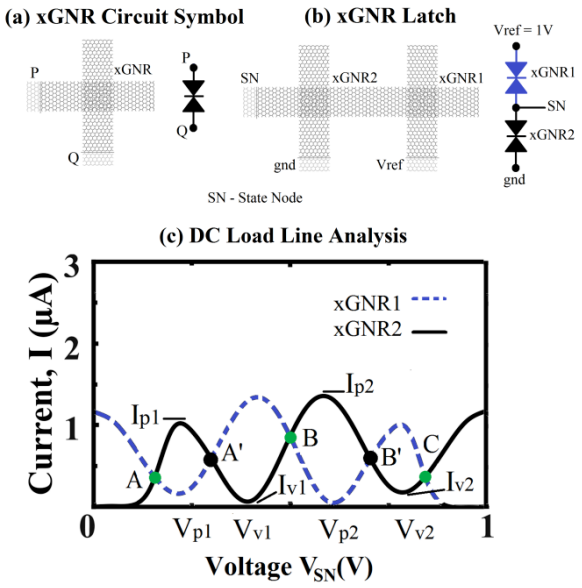

Figure 3. (a) xGNR Circuit Symbol, (b) xGNR Latch, and (c) Load Line Analysis showing multiple stable states.

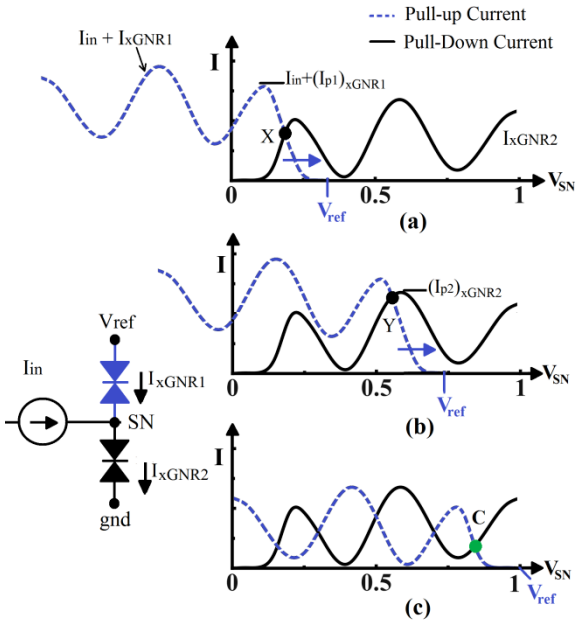

Figure 4. Load Line Analysis of xGNR latch when latching logic high. (a) & (b) Input logic high and V_{SN} at decision points, (c) Input switched off and Logic high latched.

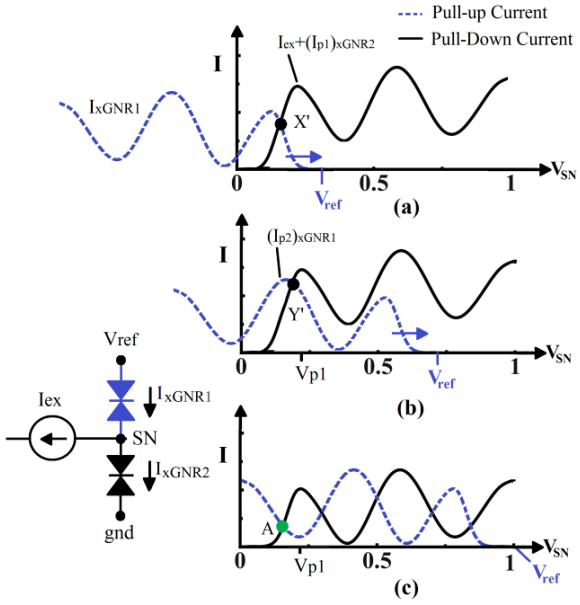

Figure 5. Load Line Analysis of xGNR latch when latching logic low - (a) & (b) Input logic low and VSN at decision points, (c) Input switched off and Logic low latched.

C. *xGNR Latch Operating Principle*

The latching mechanism, which implements an idea based on early Resonant Tunneling Diodes (RTDs) [36], can be explained using load line analysis. In the latch configuration (Fig.3), xGNR1 is connected to the reference voltage (V_{ref}) and acts as a pull-up device. The xGNR2 is connected to ground and acts as the pull-down device. The common terminal of the two devices is the *state-node* (SN) which stores the bit. The following terms will be used in the analysis –

I_{p1}, V_{p1} – First peak current and corresponding voltage

I_{p2}, V_{p2} – Second peak current and corresponding voltage

I_{v1}, V_{v1} – First valley current and corresponding voltage

I_{v2}, V_{v2} – Second valley current and corresponding voltage

Fig.4a-4c depicts the operation of latching logic 1 onto the state node by injecting currents into the latch (I_{in}). Y-axis represents current flowing through the state-node and X-axis is the voltage of state node (V_{SN}). The solid line represents pull-down current and dashed line represents pull-up currents. Assuming the state node is initially at 0, as the reference voltage V_{ref} is increased from 0, the operating point (shown by the dot X in Fig.4) is the intersection between pull-up and pull-down currents (satisfying Kirchoff's Current Law). Fig 4a shows the situation when the first pull-down current peak is encountered, called a decision point. As long as the pull-up current (I_{in} + I_{xGNR1}) is greater than pull-down current (I_{xGNR2}), the state node continues to shift from operating point X (Fig. 4a), to point Y (Fig. 4b) and finally to point C (Fig. 4c) when V_{ref} reaches 1V. When the input current is switched off, the state node is latched to logic high. Hence to be able to latch the state-node to logic 1, the following condition should be met–

$$I_{in} + (I_{p1})_{xGNR1} > (I_{p2})_{xGNR2}$$

Fig 5a-5c shows the process of latching logic 0 onto the state node. Consider the state-node is initially at 0 and the input is logic low. In this case, pull-down current (I_{ex}) exists at the state node. The analysis proceeds on the same lines as before. As long as the pull-up current (I_{xGNR1}) is lower than pull-down currents (I_{ex} + I_{xGNR2}), the state node voltage (V_{SN}) never rises beyond V_{p1} (Fig. 5b-5c). After I_{ex} is switched-off, the state node

remains at stable point A. Thus, to be able to latch logic 0, the following condition has to be satisfied –

$(I_{p2})_{xGNR1} < I_{ex} + (I_{p1})_{xGNR2}$

When used as a multi-state latch, the state node can be latched to the stable point B (in Fig. 3) if the following condition is satisfied –

$(I_{p2})_{xGNR2} > I_{in} + (I_{p1})_{\text{xGNR1}} > (I_{p1})_{xGNR2}$

When the state node is at one of the stable points (A, B or C in Fig. 3), any external disturbance that causes the state voltage to increase or decrease would be countered by strong restoring currents [37]. Points A' and B' are astable and would continue to move towards either of the surrounding stable points depending on the direction of voltage shift. For correct latch operation at stable points, the noise currents should be less than the restoring currents.

$I_{noise} < I_{p1} - I_{v2}$ (worst case)

III. Proposed GNT RAM Cell

The xGNR latch can be used in volatile random access memory. Memory-cell selection, read and write operations can be performed using access transistors similar to the RAM cell proposed in [38]. However, due to static tunneling currents through the xGNR devices, the stand-by power consumption would be considerably high (in the order of µW) when the xGNRs are always powered.

We propose a low-power xGNR based Tunneling RAM (GNT-RAM) which uses two of the stable states shown in Fig. 3 (A – logic 0 and C – logic 1) to store binary data. GNT RAM (Fig. 6) uses two xGNR devices in a latch configuration, along with a write transistor and a read transistor. To mitigate stand-by power consumption, a Schottky diode and a sleep transistor is used in series with the xGNR devices as shown in (Fig. 6). This requires the bit to be stored on a state capacitor (C_{SN}) during idle periods. The purpose of the Schottky diode is to provide current rectification during stand-by phase, by preventing reverse current flow away from the state node when logic 1 is stored on the state capacitor.

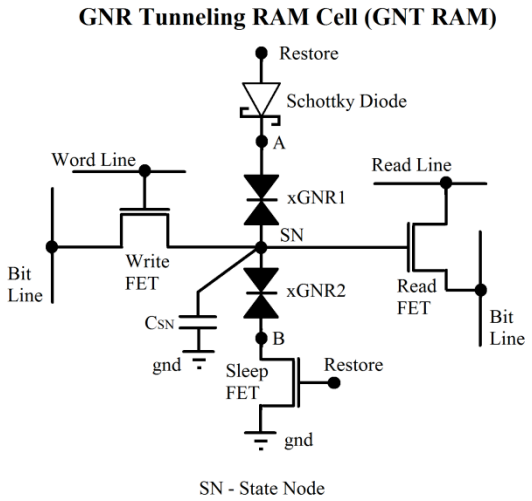

Figure 6. Proposed GNT RAM Schematic.

A. Write Operation

Consider the state node is initially at logic 0. During the start of a write operation, the 'restore' signal is initially switched-off to prevent xGNRs from contesting the change in the state node. The memory cell in which the bit is to be written is selected by applying the 'word' signal and the bit is asserted onto the 'bit line'. When logic 1 is being written, the state node is pulled-up by the write transistor and the state capacitor starts charging up. Once it reaches a voltage level which is close to logic 1 (Point 'C' in Fig. 3), the 'restore' signal is applied. This enhances the write operation by supplying restoring currents that pull the state node towards stable point 'C'. After the bit has been written, the bit-line and write signals are de-asserted while restore signal is still ON. This prevents FET switching noise transients from affecting the state node. Once the write FET is completely switched-OFF, restore signal can be de-asserted and the bit is held on the state capacitor. Due to threshold voltage drop when passing logic 1, the write NMOS FET needs to be operated at a higher than nominal voltage to ensure that the state node rises to a logic high.

Writing logic 0 onto the state node follows the same procedure, with the difference being that the bit line is now held low when the write signal is applied. This discharges the state capacitor and when the restore signal is applied, logic 0 is latched onto the state node as outlined in the xGNR latch operation in Section II.

B. Read Operation

The bit line is discharged first and the 'restore' signal is applied. The cell to be read is selected by applying the 'read' signal. If the state node is at logic 0, the read FET remains switched OFF and the bit-line remains at logic 0. If the state node is at logic 1, then the read FET is switched ON and the bit-line is pulled up. After reading, the read signal is de-asserted while the restore signal is still switched ON. After the read FET is completely switched-OFF, the restore signal is de-asserted ensuring that FET switching transients do not affect the state node. Thus, the read operation is non-destructive.

GNT RAM exploits the behavior that during a given period of time, the activity of a cache is mostly centered on a fixed number of words. Thus a major part of the memory is in idle state during which the stored value starts to leak. The application of restore signal ensures that the state node is brought back to the stable point during these idle periods. Therefore this operation does not require a read to be performed since a restoration event occurs irrespective of the logic level being stored. Hence GNT RAM can be characterized as '*quasi-static*'.

IV. Proposed Cross-Technology Layout

We propose 3-D multi-layered cross-technology integration between CMOS and graphene. The transistors are implemented using CMOS technology at the bottom, followed by a Graphene layer on top, which implements Graphene Nano-Ribbon crossbars (xGNRs). Interfacing between CMOS and Graphene layers is achieved using metal vias. The nature of the

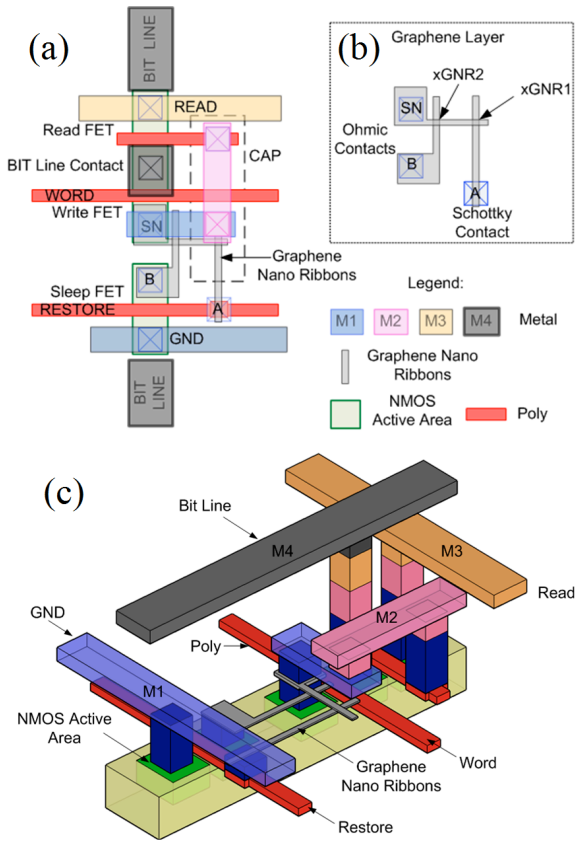

Figure 7. Proposed Graphene-CMOS Fabric - (a) Layout Top View, (b) Graphene Layer, (c) 3D Integration between CMOS and Graphene.

contact depends on the nature of GNRs. Thin semiconducting GNRs form Schottky contact with metals [39][40] and this can be exploited to realize the Schottky diode, while wide GNRs are metallic [41] and can form Ohmic contacts [40]. The physical contact resistance for the Ohmic contacts can be reduced by using a graphitic interfacial layer [42]. Routing is implemented using metal layer stack on top of the graphene layer similar to conventional CMOS.

The 3D integration between Graphene Nanoribbons and CMOS is shown in Fig 7. A uniform grid-based manufacturing-friendly layout is chosen to implement the GNT RAM. All transistors are minimum-sized NMOS FETs and are aligned in a single track. Three GNRs arranged in a crossbar implement the xGNR latch in the graphene layer. A capacitive trench can be used to implement the capacitance at the state node [43] [44]. A single bit-line is multiplexed for bit input during write and bit output during read.

V. Methodology and Simulation

Simulation was carried out using HSpice. The xGNR devices were modeled as piece-wise linear voltage controlled current sources, based on current-voltage data points. A generic integrated circuit Schottky diode model was used for first order analysis and low power 16nm CMOS PTM models [45] were used to simulate the FETs. The value of the state capacitance

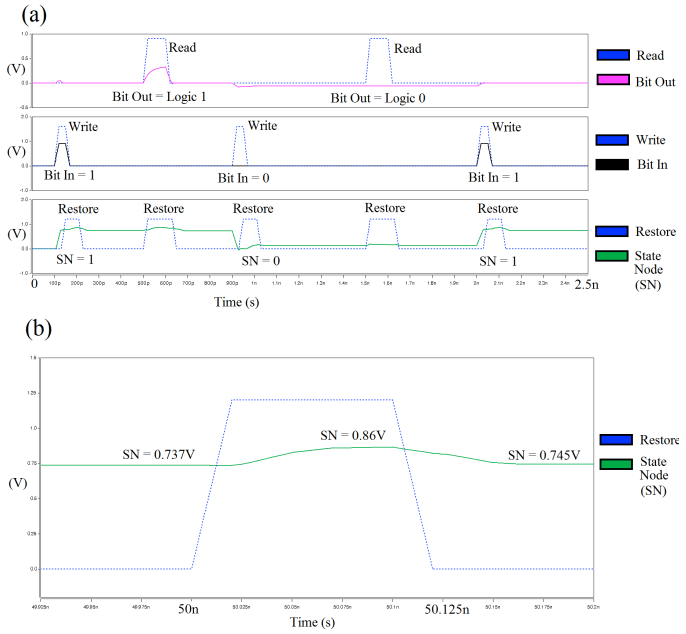

Figure 8. Simulation Waveforms for GNT RAM Operation (a) Write and Read operations, (b) Restore operation.

depends on the voltage level to be stored during stand-by. It was found that 150aF capacitance was sufficient at the state node to hold the state voltage at 0.74V during stand-by, after logic 1 is written. This ensures that when a restore signal is applied, the state node is brought up to stable point (0.86V).

The simulation waveforms for write and read operations are shown in Fig. 8a. The state node is initialized to 0 and logic 1 is first written and then read. After this, logic 0 is written followed by read. Logic 1 is written again and restore signal is applied at 50ns to verify restore operation, as shown in Fig.8b. The circuit operated as outlined in Section III.

1-D Gridded design rules [46] were used to evaluate and compare the area of GNT RAM with Gridded 8T SRAM cell [47] in 16nm technology node. In order to compare with regular 6T CMOS SRAM, a wide range of design rules were considered based on experimental data published by the industry and scaling factors across technology nodes were determined for each parameter (such as metal pitch spacing, etc.) as outlined in [48]. This evaluation methodology resulted in a range of values for interconnect dimensions and 6T SRAM cell area. PTM RC models [45] based on scaled interconnect dimensions and low power PTM transistor models [45] were used for simulation with HSpice for power and performance evaluation of 16nm CMOS 6T SRAM and Gridded 8T SRAM. Table I shows the design rules used and Table II shows the comparison results.

TABLE I. Design Rules

1D Gridded Design [46]	*M1, M2 Interconnect*	*Poly*
Pitch (16nm technology node)	40~60 nm	60~80nm

TABLE II. GNT RAM COMPARISON

		GNT RAM Cell	*16nm CMOS 6T SRAM Cell*	*16nm CMOS Gridded 8T SRAM Cell*
Area Comparison (μm^2)		0.028-0.0594	0.026-0.064	0.0336-0.0672
Power Comparison	Active Power *(μW)*	0.92-0.93	1.43-1.5	1.5-1.6
	Stand-by Power *(pW)*	52-55	125.35-125.84	78.17-79.085
Performance	Read Operation *(ps)*	24-26	10.48-11.39	9.48-9.6
	Write Operation *(ps)*	27-28	65.75-68.83	55.59-62.74

VI. RESULTS

A. Area Evaluation

GNT RAM showed a density advantage of up to 20% over 16nm CMOS 8T Gridded SRAM, and has comparable area to 16nm regular 6T SRAM cell. The area overhead in GNT RAM is due to routing and state capacitance.

B. Power Evaluation

Active power dissipation of GNT RAM was 1.55x-1.6x lower than regular 6T CMOS SRAM and 1.63x-1.72x lower than Gridded 8T CMOS SRAM cell. In terms of stand-by power dissipation, GNT RAM was 1.43x-1.5x lower than Gridded 8T SRAM and 2.28x-2.41x lower than 6T CMOS SRAM cell.

C. Performance Evaluation

In terms of performance, the write operation for GNT RAM is faster than that of SRAM mainly because the write transistor operates at a higher than nominal voltage. The read time of GNT RAM suffers due to three reasons–

- The read FET operates at lower than nominal voltage since the state node stable point for logic high is 0.86V.
- The Bit line capacitance is higher for GNT RAM due to larger cell height.
- GNT RAM uses minimum sized transistors.

VII. CONCLUSION

A novel Graphene NanoRibbon crossbar (xGNR) exhibiting negative differential resistance (NDR) was introduced and xGNR based Tunneling RAM (GNT RAM) was proposed with 3D cross technology implementation between CMOS and Graphene. It was evaluated in terms of power, performance and area and compared to 16nm CMOS 6T SRAM and 8T Gridded SRAM cell designs. GNT RAM showed considerable advantages in terms of power dissipation, area and write performance. This paper takes the initial step towards hybrid integration between CMOS and Graphene. As Graphene technology matures, future work would look at multi-state memory and a fabric with all-Graphene devices to harness the potential benefits of Graphene's extra-ordinary properties.

REFERENCES

[1] Teng Wang, Mahmoud Ben-Naser, Yao Guo, Csaba Andras Moritz, "Wire-streaming processors on 2-D nanowire fabrics", NSTI (Nano Science and Technology Institute) Nanotech 2005, California, May 2005.

[2] C. A. Moritz, P. Narayanan, and C. O. Chui, "Nanoscale application specific integrated circuits." Nanoelectronic Circuit Design. 1st ed. Niraj K. Jha and Deming Chen, New York: Springer, 2011. 215-76.

[3] P.Panchapakeshan, P.Narayanan, C.A.Moritz, "N3ASICs: Designing nanofabrics with fine-grained CMOS integration," Nanoscale Architectures (NANOARCH), 2011 IEEE/ACM International Symposium on, in press.

[4] Shabadi, P.; Khitun, A.; Narayanan, P.; Mingqiang Bao; Koren, I.; Wang, K.L.; Moritz, C.A.; , "Towards logic functions as the device," Nanoscale Architectures (NANOARCH), 2010 IEEE/ACM International Symposium on , vol., no., pp.11-16, 17-18 June 2010.

[5] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, M. I. Katsnelson, I. V. Grigorieva, S. V. Dubonos, and A. A. Firsov, "Two-dimensional gas of massless dirac fermions in graphene," Nature, vol. 438, no. 7065, pp. 197–200, November 2005.

[6] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grig-orieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," Science, vol. 306, no. 5696, pp. 666–669, 2004.

[7] Schwierz, Frank. "Graphene transistors." Nature Nanotechnology 5.7 (2010): 487-96.

[8] T. Ando, "Exotic electronic and transport properties of graphene," Physica E: Low-dimensional Systems and Nanostructures, vol. 40, no. 2, pp. 213 – 227, 2007.

[9] X. Li, X. Wang, L. Zhang, S. Lee, and H. Dai, "Chemically derived, ultrasmooth graphene nanoribbon semiconductors," Science, vol. 319, no. 5867, pp. 1229–1232, 2008.

[10] K.-T. Lam and G. Liang, "An ab initio study on energy gap of bilayer graphene nanoribbons with armchair edges," Applied Physics Letters, vol. 92, no. 22, p. 223106, 2008.

[11] C. L. Lu, C. P. Chang, Y. C. Huang, J. M. Lu, C. C. Hwang, and M. F. Lin, "Low-energy electronic properties of the ab-stacked few-layer graphites," Journal of Physics: Condensed Matter, vol. 18, no. 26, p. 5849, 2006.

[12] H. Min, B. Sahu, S. K. Banerjee, and A. H. MacDonald, "Ab initio theory of gate induced gaps in graphene bilayers," Phys. Rev. B, vol. 75, no. 15, p. 155115, Apr 2007.

[13] Y. Zhang, T.-T. Tang, C. Girit, Z. Hao, M. C. Martin, A. Zettl, M. F. Crommie, Y. R. Shen, and F. Wang, "Direct observation of a widely tunable bandgap in bilayer graphene," Nature, vol. 459, no. 7248, p. 820, 2009.

[14] G. Fiori and G. Iannaccone, "On the Possibility of Tunable-Gap Bilayer Graphene FET," IEEE Electron Device Letters, vol. 30, no. 3, pp. 261–264, March 2009.

[15] Fiori, G.; Iannaccone, G.; "Ultralow-Voltage Bilayer Graphene Tunnel FET," IEEE Electron Device Letters, vol. 30, no. 10, pp. 1096–1098, Oct 2009.

[16] K.-T. Lam and G. Liang, "A computational evaluation of the designs of a novel nanoelec-tromechanical switch based on bilayer graphene nanoribbon," in IEEE Int. Electron Devices Meeting Tech. Dig. New York: IEEE, 2009, pp. 37.3.1 – 37.3.4.

[17] K.-T. Lam, C. Lee, and G. Liang, "Bilayer graphene nanoribbon nanoelectromechanical system device: A computational study," Applied Physics Letters, vol. 95, no. 14, p. 143107, 2009.

[18] S. K. Banerjee, L. F. Register, E. Tutuc, D. Reddy, and A. H. MacDonald, "Bilayer pseudospin field-effect transistor (bisfet): A

proposed new logic device," IEEE Elect. Dev. Lett., vol. 30, no. 2, pp. 158 – 160, 2009.

[19] H. Ren, Q.-X. Li, Y. Luo, and J. Yang, "Graphene nanoribbon as a negative differential resistance device," Applied Physics Letters, vol. 94, no. 17, p. 173110, 2009.

[20] V. N. Do and P. Dollfus, "Negative differential resistance in zigzag-edge graphene nanoribbon junctions," Journal of Applied Physics, vol. 107, no. 6, p. 063705, 2010.

[21] K. M. M. Habib, F. Zahid and R. K. Lake, "Negative differential resistace in bilayer graphene nanoribbons," Applied Physics Letters (in review).

[22] K. M. M. Habib and R. K. Lake, "Graphene nanoribbon crossbar resonant tunneling diode," (in preparation).

[23] O. F. Sankey and D. J. Niklewski, "Ab initio multicenter tight-binding model for molecular-dynamics simulations and other applications in covalent systems," Phys. Rev. B, vol. 40, no. 6, pp. 3979 – 3995, 1989.

[24] J. P. Lewis, K. R. Glaesemann, G. A. Voth, J. Fritsch, A. A. Demkov, J. Ortega, and O. F. Sankey, "Further developments in the local-orbital density-functional-theory tight-binding method," Phys. Rev. B, vol. 64, no. 19, p. 195103, 2001.

[25] Y.-W. Son, M. L. Cohen, and S. G. Louie, "Energy gaps in graphene nanoribbons," Phys. Rev. Lett., vol. 97, no. 21, p. 216803, 2006.

[26] J. L. Martins, N. Troullier, and S. H. Wei, "Pseudopotential plane-wave calculations for ZnS," Phys. Rev. B, vol. 43, no. 3, pp. 2213 – 2217, 1991.

[27] A. D. Becke, "Density-functional exchange-energy approximation with correct asymptotic behavior," Phys. Rev. A, vol. 38, no. 6, pp. 3098 – 3100, 1988.

[28] C. Lee, W. Yang, and R. G. Parr, "Development of the colle-salvetti correlation energy formula into a functional of the electron density," Phys. Rev. B, vol. 37, no. 2, pp. 785 – 789, 1988.

[29] J. Harris, "Simplified method for calculating the energy levels of weakly interacting fragments," Phys. Rev. B, vol. 31, pp. 1770–1779, 1985.

[30] W. M. C. Foulkes and R. Haydock, "Tight-binding models and density-functional theory," Phys. Rev. B, vol. 39, pp. 12 520–2536, 1989.

[31] A. A. Demkov, J. Ortega, O. F. Sankey, and M. P. Grumbach, "Electronic structure approach for complex silicas," Phys. Rev. B, vol. 52, no. 3, pp. 1618 – 1630, 1995.

[32] P. Jelinek, H. Wang, J. P. Lewis, O. F. Sankey, and J. Ortega, "Multicenter approach to the exchange-correlation interactions in ab initio tight-binding methods," Phys. Rev. B, vol. 71, no. 23, p. 235101, 2005.

[33] N. A. Bruque, M. K. Ashraf, T. R. Helander, G. J. O. Beran, and R. K. Lake, "Conductance of a conjugated molecule with carbon nanotube contacts," Phys. Rev. B, vol. 80, no. 15, p. 155455, 2009.

[34] N. A. Bruque, R. R. Pandey, and R. K. Lake, "Electron transport through a conjugated molecule with carbon nanotube leads," Phys. Rev. B, vol. 76, no. 20, p. 205322, 2007.

[35] Mazumder, P.; Kulkarni, S.; Bhattacharya, M.; Jian Ping Sun; Haddad, G.I.; , "Digital circuit applications of resonant tunneling devices," Proceedings of the IEEE, vol.86, no.4, pp.664-686, Apr 1998.

[36] Williamson, W., III; Enquist, S.B.; Chow, D.H.; Dunlap, H.L.; Subramaniam, S.; Peiming Lei; Bernstein, G.H.; Gilbert, B.K.; , "12 GHz clocked operation of ultralow power interband resonant tunneling diode pipelined logic gates," Solid-State Circuits, IEEE Journal of , vol.32, no.2, pp.222-231, Feb 1997.

[37] van der Wagt, J.P.A.; , "Tunneling-based SRAM," Proceedings of the IEEE , vol.87, no.4, pp.571-595, Apr 1999

[38] van der Wagt, J.P.A.; Seabaugh, A.C.; Beam, E.A., III.; , "RTD/HFET low standby power SRAM gain cell," Electron Device Letters, IEEE , vol.19, no.1, pp.7-9, Jan 1998.

[39] Ling-Feng Mao; Li, X.J.; Zhu, C.Y.; Wang, Z.O.; Lu, Z.H.; Yang, J.F.; Zhu, H.W.; Liu, Y.S.; Wang, J.Y.; , "Finite-Size Effects on Thermionic Emission in Metal–Graphene-Nanoribbon Contacts," Electron Device Letters, IEEE , vol.31, no.5, pp.491-493, May 2010.

[40] Ximeng Guan; Qiushi Ran; Ming Zhang; Zhiping Yu; Wong, H.-S.P.; , "Modeling of schottky and ohmic contacts between metal and graphene nanoribbons using extended hückel theory (EHT)-based NEGF method," Electron Devices Meeting, 2008. IEDM 2008. IEEE International , vol., no., pp.1-4, 15-17 Dec. 2008.

[41] Unluer, D.; Tseng, F.; Ghosh, A.; Stan, M.; , "Monolithically patterned wide-narrow-wide all-graphene devices," Nanotechnology, IEEE Transactions on , vol.PP, no.99, pp.1, 0.

[42] Yang Chai; Hazeghi, A.; Takei, K.; Hong-Yu Chen; Chan, P.C.H.; Javey, A.; Wong, H.-S.P.; , "Graphitic interfacial layer to carbon nanotube for low electrical contact resistance," Electron Devices Meeting (IEDM), 2010 IEEE International, vol., no., pp.9.2.1-9.2.4, 6-8 Dec. 2010.

[43] J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuits – A Design Perspective", 2nd Edition, Prentice Hall, NJ, 2003.

[44] Pritish Narayanan, Jorge Kina, Pavan Panchapakeshan, Chi On Chui, and Csaba Andras Moritz, "Integrated device-fabric explorations and noise mitigation in nanoscale fabrics", Submitted to TNANO under review.

[45] Predictive Technology Model, http://ptm.asu.edu/

[46] C. Bencher, H. Dai, and Y. Chen. "Gridded design rule scaling: Taking the CPU toward the 16nm node", Proc. SPIE 7274, 2009.

[47] R. T Greenway, K. Jeong and A. B. Kahng, C.-H. Park and J. S. Petersen, "32nm 1-D regular pitch SRAM bitcell design for interference-assisted lithography", Proc. SPIE BACUS, 2008.

[48] Mostafizur Rahman, Pritish Narayanan, and Csaba Andras Moritz, "N3ASIC-based nanowire volatile RAM" 11th IEEE Nanotechnology conference (NANO 2011), in press.