

# A Wafer-scale Manufacturing Pathway for Fine-grained Vertical 3D-IC Technology

## Abstract

Three-dimensional integrated circuits (3D-ICs) provide a feasible path for scaling CMOS technology in the foreseeable future. IMEC and IRDS roadmaps project that 3D integration is a key avenue for the IC industry beyond 2024. They project that some form of 3D-IC technology based on nanosheets/nanowires is likely to become mainstream soon. SkyBridge-3D-CMOS (S3DC) is one among the first vertical nanowire-based fine-grained 3D-IC directions which offers paradigm shift in technology scaling as well as design. Rather than die-die and layer-layer stacking, S3DC's core aspects, from device to circuit style to interconnect, are co-architected in a 3D fabric-centered manner building on a uniform 3D nanowire template. Nanowire-based 3D-IC technologies such as S3DC solve most of the traditional scaling issues of 2D-CMOS but present new manufacturing challenges because of their complex 3D geometry. Therefore, for these directions to become mainstream, a robust wafer-scale manufacturing pathway that addresses these challenges is vital. In this paper, we propose a wafer-scale manufacturing pathway aimed at developing and optimizing the manufacturing process flows of S3DC. Using physics-driven virtual process integration functionalized with design and process parameters, we obtained realistic 3D structures for all the underlying IC elements and finally combined them to build 3D standard cells in S3DC. Electrical characterization of resultant structures using process and device simulations were performed while considering the material properties and nanoscale physics effects. Circuit-level simulations accounting for device behavior using SPICE-compatible compact model and circuit interconnect parasitics were carried out to study the impact of variations in process steps such as patterning, lithography, etch, deposition on device and interconnect performance. Our bottom-up simulation results indicate that the proposed pathway is robust enough to be adopted for large-scale production thus paving the way for wide-spread adoption of vertical fine-grained 3D-IC technologies.

## Keywords

3D integrated circuits, virtual fabrication, vertical 3D-IC

## 1. Introduction

Continuous scaling of CMOS has been the key driver of miniaturization of integrated circuits (ICs). Moving forward, traditional scaling will have significant challenges as MOSFETs are reaching their fundamental limits and interconnection bottleneck is dominating IC operational power and performance [1]. Three-Dimensional (3D) integration is likely to play a major role in overcoming many of these scaling limitations. Recently, Monolithic-3D (M3D) and Parallel-3D (P3D) have emerged as promising 3D-IC directions [2][3]. Monolithic-3D is a layer-to-layer stacking approach where nanoscale vias are used for connectivity between the layers whereas Parallel-3D involves die-to-die stacking with connectivity achieved by Through-Silicon-

Vias (TSVs). In addition to suffering from traditional scaling challenges such as regional 3D doping and routability, these approaches are also plagued by customization and manufacturing requirements that are incompatible with fine-grained 3D organization.

In recent years there have been research efforts toward developing novel fine-grained 3D-IC directions [4][5] which offer paradigm shift in technology scaling as well as design. In contrast to 2D-CMOS, that has evolved focusing on the device scaling and requires a largely component-centric assembly, these approaches shift to a fabric-centric mindset and provide an integrated solution for all technology aspects. These approaches use gate-all-around (GAA) devices and 3D interconnect structures amenable for vertical integration making them fundamentally different from 2D-CMOS. First among such approaches is SkyBridge-3D-CMOS (S3DC) [4], a vertically composed fine-grained CMOS 3D-IC technology. Such fabrics are more naturally amenable to scaling to sub-5nm technology node. S3DC has been extensively evaluated in all the relevant benchmarking metrics such as performance, power, area, routability and is shown to have significant benefits when compared to 2D-CMOS, M3D and P3D [4]. Furthermore, several key fabric elements including the gate-all-around (GAA) junctionless transistor was experimentally demonstrated. Moving forward, wafer-scale manufacturability is the crucial step in making it and similar vertical 3D-IC technologies mainstream.

S3DC's manufacturing pathway is based on multi-layer material deposition to functionalize the nanowire template to form 3D GAA transistors, contacts, and interconnect [5]. The critical dimensions of the devices and contact are not defined by high-resolution lithography but simply by the thickness of deposited material. Hence, lithographic precision is required only for patterning of nanowires. Furthermore, it does not involve selective doping process as the doping is done once at a wafer level. Several key fabric elements of S3DC including the gate-all-around (GAA) junctionless transistor have already been experimentally demonstrated [5]. However, wafer-scale manufacturing of S3DC presents new set of challenges. Some of these challenges include ensuring regularity in nanowire pattern density, achieving uniformity in nanowire thickness, uniformity in gate definition of GAA devices, photoresist and inter-layer dielectric planarization, among others. Previously, fabs had to rely on thousands of testing cycles on wafers before converging on a robust manufacturing flow. However, continuous technology scaling has resulted in increased complexity leading to increase in cost and time. Recently, semiconductor manufacturing industry has adopted virtual fabrication techniques by emulation of hundreds of processes typically involved in large-scale manufacturing. Computer-aided Design (CAD) tools specifically built for this purpose support physical etch and deposition process models which can be tuned by behavioral parameters to obtain fine control over the resultant structures. Hence, for any new IC technology, virtual

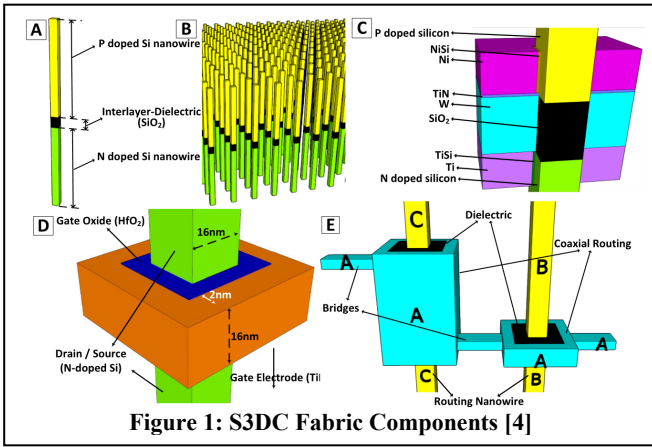


Figure 1: S3DC Fabric Components [4]

process flows are crucial for process integration engineers to gain valuable insights before proceeding to the wafer testing phase. As the industry looks to adopt 3D-IC technology for the next-gen chips, process emulation of key manufacturing steps is critical.

In this paper, we present a wafer-scale manufacturing pathway for S3DC derived by physics-driven virtual process integration. Using a state-of-the-art process emulation tool, Synopsys Sentaurus Process Explorer R-2020.09, we developed and optimized the process flows using industry-proven unit processes to obtain fab-realistic 3D models of standard cells in S3DC. We performed detailed IV and CV characterization of the resultant device structures using Synopsys TCAD Sentaurus Process and Device R-2020.09 simulators while considering manufacturing imperfections imparted by the unit processes during the process flow. To validate our pathway, we performed extensive circuit simulations of process-derived 3D standard cells and investigated the effects of process variation on their behavior, performance, and power. The circuit-level simulations of standard cells were enabled by SPICE-compatible compact model and layout RC parasitics extracted directly from structures obtained after process emulations.

The rest of the paper is organized as follows. In Section 2, we provide background for S3DC technology. In Section 3, we present CAD flow. Section 4 describes the wafer-scale manufacturing flow. In Section 5, we present the process and device simulation results. Section 6 describes compact modeling and RC parasitic extraction. Section 7 details our variability analysis. Section 8 concludes the paper.

## 2. SkyBridge-3D-CMOS Fabric

SkyBridge-3D-CMOS (S3DC) is a vertically composed fine-grained 3D IC technology, designed with a 3D fabric-centric mindset and providing an integrated solution for all core technology challenges [4]. It is the first fine-grained 3D-CMOS IC technology leveraging the vertical dimension. Fig.1 shows S3DC fabric components; it is built with a regular array of uniform vertical dual-doped nanowires (See Fig.1A, 1B); all active components and structures are vertically composed by selective material deposition around nanowires. Active devices are placed and connected on these nanowires either in series (on one nanowire) or in parallel (across multiple nanowires connected in parallel) to

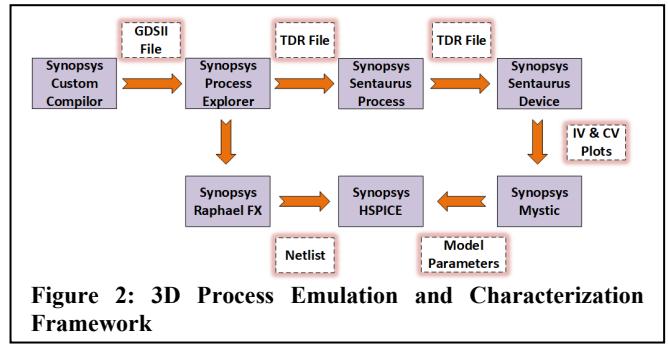


Figure 2: 3D Process Emulation and Characterization Framework

build CMOS circuits. Vertical Gate-All-Around (V-GAA) junctionless transistors are the active devices in S3DC. An n-type V-GAA junctionless transistor structure is shown in Fig.1D. The source, channel, and drain regions are based on heavily doped vertical nanowires. Carefully selected gate electrodes and dielectric materials are surrounding the nanowire. The V-GAA behavior is modulated by the work function difference between gate and channels. SkyBridge Interlayer-Connection (SB-ILC) is the specially designed structure that connects the p-type pull-up and n-type pull-down networks together to generate the output signal. The SB-ILC structure is shown in Fig.1C. Routing nanowires are vertical nanowires (Fig.1E) that are silicided, thus having low resistivity. Routing Bridges (Fig.1E) are horizontal metal wires connecting adjacent nanowires. Coaxial Routing structures (Fig.1E) are metal layers formed along the vertical routing nanowires (with insulating oxide ring) to add connectivity in vertical direction. All the circuit design and layout in S3DC adhere to 3D specific design rules and guidelines.

## 3. CAD Flow

Sentaurus Process Explorer R-2020.09, a state-of-the-art process emulations tool, is used to build a full set of virtual process decks. It provides an extensive set of physical deposition and etch models whose behavioral parameters can be tuned to get realistic structures. It provides fine control over behavioral process parameters such as deposition and etch rates, local density variation, degree of anisotropy, conformity of deposition etc. It also provides process steps to emulate advanced processes such as Atomic Layer Deposition (ALD) and Atomic Layer Etching (ALE).

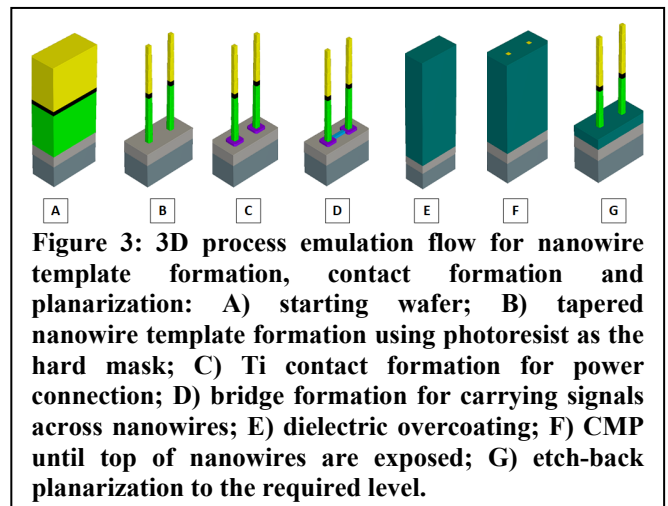
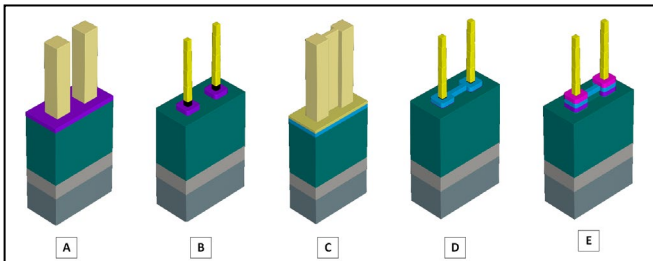


Figure 3: 3D process emulation flow for nanowire template formation, contact formation and planarization: A) starting wafer; B) tapered nanowire template formation using photoresist as the hard mask; C) Ti contact formation for power connection; D) bridge formation for carrying signals across nanowires; E) dielectric overcoating; F) CMP until top of nanowires are exposed; G) etch-back planarization to the required level.

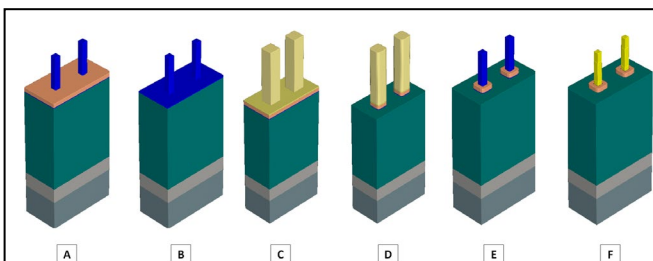


**Figure 4: 3D process emulation flow for ILC formation:** A) lithography to define the Ti contacts; B) anisotropic etching to remove excess Ti; C) lithography to define bridge between the ILC; D) anisotropic etching of Tungsten to define bridges; E) ILC with bridge.

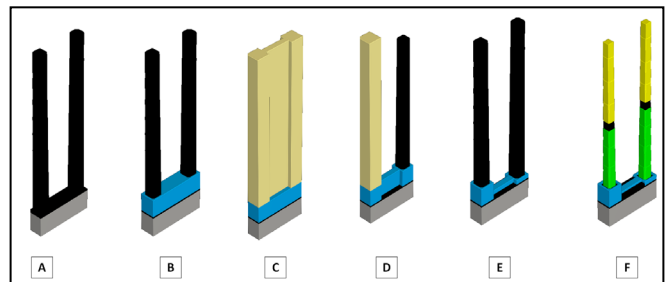
Furthermore, it provides live 3D interactive visualizations of the structures as the process deck is being developed. Synopsys Custom Compiler R-2020.09 is used to draw 2D layouts required for defining the masks for the lithography steps during the process emulation. The 3D models are then sent to Synopsys TCAD Sentaurus Process R-2020.09 for process simulations such as doping, meshing and contact generation. After process simulations, the models are sent to Synopsys TCAD Sentaurus Device R-2020.09 to obtain the electrical properties of the fabric components. The IV and CV characteristics obtained from the device simulations are sent to Mystic R-2020.09 tool for development of BSIM-CMG based compact model. The same 3D structures obtained after process emulation are sent to Synopsys Raphael FX R-2020.09 for extracting 3D layout-specific RC parasitic netlist. The compact model and parasitic RC netlist are combined to generate standard cell netlists which are used in HSPICE simulations. Fig. 2 shows the block diagram of the framework.

#### 4. S3DC Wafer-scale Manufacturing Flow

**Wafer Preparation:** Vertical GAA transistors do not require abrupt doping variations within the device; as a result, complexities related to precision doping in 3D and high temperature annealing are eliminated. A wafer-level *a priori* doping is sufficient for devices and contacts. Wafer preparation involves stacking heavily doped n-type and p-type crystalline silicon layers to create a dual-doped silicon



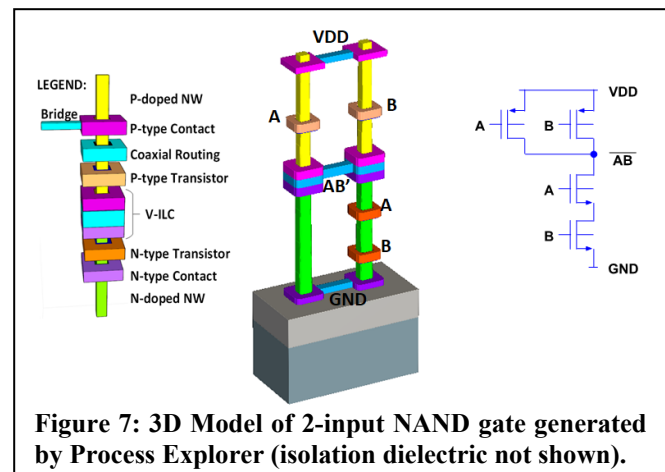
**Figure 5: 3D process emulation of p-type GAA transistors:** A) anisotropic deposition of Tungsten Nitride for gate electrodes; B) isotropic deposition of high-k dielectric (HfO<sub>2</sub>); C) UV Lithography to define gate electrodes; D) anisotropic etching of Tungsten Nitride resulting in rounded corners; E) photoresist striped to expose nanowires; F) isotropic etching of gate dielectric.



**Figure 6: 3D process emulation flow for coaxial routing structure with bridge:** A) isotropic deposition of silicon dioxide around nanowires for isolation; B) anisotropic deposition of Tungsten; C) lithography to define the bridge between the co-axial routing structures; C) lithography to etch Tungsten to the required level; D) anisotropic etching of Tungsten; C) Isotropic etching of silicon dioxide to expose the nanowires.

substrate wafer using molecular bonding techniques and is currently used for 3D-ICs. A silicon dioxide layer is sandwiched between the n-type and p-type doped silicon layers for isolation. Noticeably, unlike conventional CMOS technology, doping is required only once prior to any processing steps. The starting wafer contains a top 200 nm thick p-type silicon layer, 50nm thick silicon dioxide isolation layer, 200nm thick n-type silicon layer, 100nm buried oxide (SiO<sub>2</sub>) layer and 200nm bottom handle layer (Si) (see Fig. 4A).

**Nanowire Template Formation:** Patterning of arrays of high aspect ratio vertical nanowires is the next step in the manufacturing flow. Ideally, all the nanowires have similar aspect ratio, and maintain uniform distances between each other. High aspect ratio uniform vertical nanowires with smooth surfaces can be achieved through patterning by Inductively Coupled Plasma (ICP) dry etching. ICP etch is shown to have elevated etch rates, high directionality aiding in creating anisotropic profiles required for smooth vertical sidewalls and high aspect ratio. It is routinely used in etching of high aspect ratio silicon fins in the FinFET manufacturing [6]. Furthermore, several research groups have demonstrated high aspect ratio nanowires that are in line with S3DC's requirements [4]. These groups have demonstrated nanowires of various widths ranging from 30 nm to 5 nm, the highest aspect ratio being 50:1. These



**Figure 7: 3D Model of 2-input NAND gate generated by Process Explorer (isolation dielectric not shown).**

groups have reported tapered nanowires with bottom region being slightly wider than the top. However, it is advantageous to have tapered shapes in nanowires because they allow for higher mechanical rigidity to withstand further processing steps.

A thin layer of Bottom Anti-reflective Coating (BARC) is deposited before every photoresist step. Square positive photoresist dots of 16nm are patterned on top of the wafer followed by 460 nm deep Si/SiO<sub>2</sub> anisotropic etch with 80 nm/min etch rate. No hard mask is required since photoresist such as Hydrogen Silsesquioxane (HSQ) with high mechanical strength can be used. This results in nanowires being etched until it reaches the buried oxide (see Fig. 3B). This is done to isolate the pillars from shorting the n- and p-type silicon and prevent undesired latch-up conditions. A tapered profile was replicated using unified etch model which allows tuning parameters such as anisotropy, lateral etch rate, etch angle etc. in Process Explorer. The widths at the bottom, middle and top are 32nm, 22nm and 16nm respectively, which are similar to the experimental demonstration in [7].

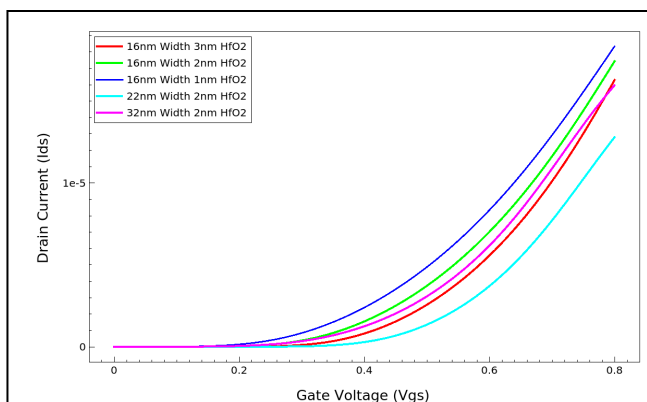
**Contact Formation:** Nanowire patterning is followed by a contact formation step for connecting the nanowire with power rails at the bottom. Ohmic contacts at different heights are also formed for input/output and power rail (VDD, GND) connections. To make an Ohmic contact, anisotropic deposition of Titanium (Ti), a widely used material for Ohmic contacts to heavily doped silicon, is performed by Chemical Vapor Deposition (CVD) followed by photoresist deposition. CVD is the most sought-after process for anisotropic deposition and is widely used in the industry. The region surrounding the nanowires is exposed using UV lithography; the region of exposure is determined by the minimum material dimension requirements for the Ohmic contact. The excessive Ti is then etched away to form the contact. The required Ti thickness and length are derived considering the lithographic alignment precision (+3.3nm at 16nm node).

Anisotropic CVD deposition model is used to deposit 10nm thick Ti followed by a patterning step using positive photoresist. After UV exposure, the photoresist acts as the hard mask and excessive Ti is etched away using anisotropic etch model (see Fig. 3C). Anisotropic etching using RIE is

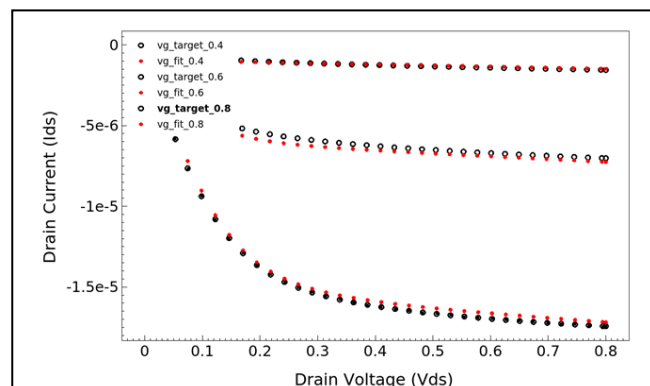
prone to imperfections. Even though it is used for vertical etching, it also results in lateral etch of structures as well. Anisotropic etch model in Process Explorer allows to configure lateral etch rates. We have considered realistic lateral etch rates from literature and used it in the etch process. Anisotropic etching also results in corner smoothing effects which was also modeled.

**Signal carrying bridges:** Manufacturing steps for input signal carrying Bridges begins with anisotropic CVD of Tungsten followed by pattern definition using photoresist. After UV exposure, the exposed resist is stripped away followed by anisotropic etching of Tungsten with resist being the etch-mask to design the bridges. Other Bridge structures such as routing Bridges follow similar methodology for fabrication. Anisotropic deposition model is used to deposit 10nm thick Tungsten. A positive photoresist is spun and after UV exposure the exposed part is stripped to pattern the bridge. Anisotropic etch model with corner rounding effects is used to etch the exposed Tungsten (see Fig. 4D). The inter-layer connection (SB-ILC) used to connect the n-type and p-type nanowires is fabricated using the combination of contact formation and bridge steps (see Fig. 5).

**Planarization:** Since S3DC's manufacturing pathway is primarily based on material deposition, each layer needs to be planarized between depositions. Chemical Mechanical Polishing (CMP) is the industry standard for planarization in the CMOS manufacturing. Another technique is to use etch-back planarization which involves over-coating the structures with dielectric materials such as SiO<sub>2</sub> or HSQ followed by a wet etch to the required level. The industry uses a combination of CMP and etch-back planarization during FinFET fabrication [8]. After the fin formation step, the fins are over-coated with SiO<sub>2</sub> using CVD. A step of CMP is performed until the topmost part of the fins are exposed and then etch-back planarization is performed until the desired height. This results in a highly planarized surface without damaging the fins. Similarly, in S3DC's manufacturing flow, we use a combination of CMP and etch-back planarization. After each material deposition step, nanowires are over-coated with Silicon-On-Glass oxide. Then CMP is used to remove excess SiO<sub>2</sub>, thus exposing the tip of the nanowire. The excess materials formed on the nanowire during material deposition steps can also be removed by CMP [9]. After this the oxide is etched back



**Figure 8: Process and Device Simulations results: A)  $I_{ds}$ - $V_{gs}$  curve showing impact of nanowire channel width and gate oxide thickness.**



**Figure 9: Compact Model Fitting Results**

using wet etching to the desired height. The combination of CMP and etch back techniques help achieve local and global planarization of the wafer surface. Alternatively, [9] demonstrated using HSQ as the dielectric material instead of SiO<sub>2</sub> for planarization. They demonstrated an extremely flat layer with roughness thickness below 2nm without degradation of HSQ or the nanowires. SOG oxide overcoating is performed to completely cover the nanowires using the SOG deposition model in Process Explorer. CMP etch model is used to perform the planarization to just expose the top of the nanowires. Then wet etch model with etch rate of 43 nm/min was used to etch the oxide to the required level (see Fig. 3E, 3F, 3G).

**Vertical GAA Transistor:** Selective gate material deposition is a key process step in S3DC assembly. High-k gate dielectric and gate electrode are deposited in selective places in the nanowire template to form GAA devices. We propose a flow which does not require high-resolution lithography step for gate dielectric deposition. In this flow, the channel length is determined by the material deposition step which can be controlled with very high precision. The key technique which enables thin deposition of gate dielectric is Atomic Layer Deposition (ALD).

The flow starts with a planarized surface followed by anisotropic deposition of 10nm thick Nickel (Ni) (Titanium for n-type device). SiO<sub>2</sub> provides the isolation between the contacts of the transistor. The source contact patterned using photoresist to etch away the excess. This is followed by an isotropic deposition of Hafnium dioxide (HfO<sub>2</sub>) for the gate oxide. Since the gate oxide deposition must be controlled to nanometer's precision, there is a room for error here which we have taken into consideration. This is followed by anisotropic deposition of 16nm Tungsten Nitride (WN) (Titanium Nitride for n-type device) for the gate electrode. The thickness of WN layer is determined both by minimum gate electrode thickness requirement for device functionality and lithographic alignment precision ( $\pm 3.3\text{nm}$  at 16nm node). This is followed by photoresist deposition and lithography to define the gate electrode. The photoresist acts as the etch mask to remove the excess WN and HfO<sub>2</sub>. After resist is stripped away, isotropic etching of HfO<sub>2</sub> is performed to remove it except under the WN to define the gate stack. A 10nm thick Ni is deposited and patterned to form the drain contact (see Fig. 5). The co-axial routing structures follow a flow similar to GAA transistors albeit with different materials (see Fig. 6).

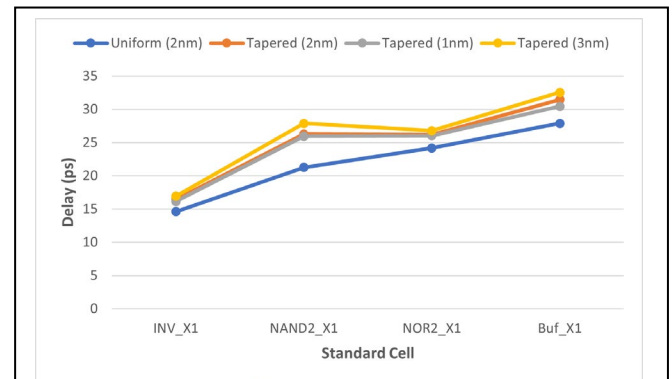
## 5. Process and Device Simulations

Sentaurus Process simulator was used for process simulation of ion implantation required for doping. To identify the annealing temperature for substrate re-crystallization, ion implantation parameters (acceleration voltage 28KeV) obtained from SRIM was used in process simulations. For the n-type, the doping concentration was  $10^{19}$  dopants/cm<sup>3</sup> and for p-type it was  $10^{20}$  dopants/cm<sup>3</sup>. Substrate annealing at 1000° C for 60 minutes in N<sub>2</sub> ambient was found to be adequate for substrate re-crystallization, and diffusion and activation of dopants. The ion implantation process was modeled using Monte Carlo (TRIM) simulation model. Diffusion and activation processes were modeled

using Charged Cluster model. Manufacturing imperfections at two different steps determine the quality of the devices obtained. First, the tapering profile of the nanowires changes the transistor channel width. Second, during isotropic deposition of very thin layer of gate oxide may not be well-controlled every time. Both situations influence device characteristics. We have accounted for both situations during electrical characterization. Fig. 8 shows I<sub>ds</sub>-V<sub>gs</sub> characteristics for different gate oxides and nanowire widths; 1nm HfO<sub>2</sub> shows superior characteristics with I<sub>on</sub>/I<sub>off</sub> of 10<sup>7</sup> compared to 3nm HfO<sub>2</sub>, which is primarily due to stronger electric field due to thinner HfO<sub>2</sub> high-k dielectric. As the channel width increases, the on current increases thus improving the performance of the transistors. However, this increases the off current as well.

## 6. Compact Modeling and RC Parasitic Extraction

To perform large-scale circuit-level simulations in S3DC, having a compact model for V-GAA is important. Compact models offer versatility without compromising ease of use and computational efficiency. BSIM-CMG [10] compact model from UC Berkeley is an industry-standard for modeling multi-gate transistors. VGAA transistors are volume inversion devices. BSIM-CMG has volume inversion included in the solution of the Poisson's equation. Hence, BSIM-CMG was used to derive compact model for VGAA transistors. To extract model parameters for the transistors, an industry-standard Mystic TCAD-to-SPICE tool from Synopsys was used. Mystic takes in IV and CV characteristics of transistors coming from TCAD, initial model card, metadata, and outputs a SPICE model card with extracted model parameters guided by an extraction optimization strategy. It provides a sleuth of local and global optimization algorithms to guide the user towards an optimal SPICE model to fit the TCAD data. The initial model card was initialized with known parameters of VGAA transistors such as channel length and width, gate metal work function, effective oxide thickness, channel doping etc. We used the bounded trust region optimization algorithm, and it gave the best results compared to other algorithms. The final fitting results for I<sub>ds</sub> vs V<sub>ds</sub> for p-type GAA transistors are shown in Fig. 9. As seen from the plots, we got a good fitting of the IV characteristics.



**Figure 10: Impact of gate oxide thickness and nanowire width variation on cell critical delay. Tapered nanowire has varying amount of HfO<sub>2</sub> thickness**

3D layout-specific RC parasitic extraction was performed using Synopsys Raphael FX. The 3D structures generated using process explorer was imported to the tool. It considers the material properties, distances between the structures etc. to generate RC netlists which can then be used in HSPICE netlists.

### 7. 3D Cell Evaluation and Analysis

**Table 1: Power Savings of tapered nanowire standard cells normalized to uniform nanowire-based standard cells.**

Cell	Tapered (1nm)	Tapered (2nm)	Tapered (3nm)
INV_X1	6%	7%	9%
NAND2_X1	9%	11%	12%
NOR2_X1	5%	6%	8%
BUF_X1	10%	12%	13%

In this section, we focus on specific sources of manufacturing imperfections related to etching, deposition processes and show their implications on standard cell benchmarking metrics: area, power, and performance. As discussed in section 5, the device behavior is mainly dependent on nanowire channel width and thickness of gate oxide. The variations in etching and deposition at contacts may affect layout RC parasitics. To this end, we built physical HSPICE netlists of several standard cells such as inverter, buffer, NAND2, NOR2, AND2, OR2, AOI21, AOI22 and a flip flop. For performance and power evaluation, we set FO4 load, which assumes that each cell has an average fan-out of four inverters. The critical delay is measured by assuming the worst-case scenario where both the inputs and outputs of the cells are switching. The measured power is average dynamic power of all switching scenarios. The power of each standard cell is measured assuming input signal frequency of 1GHz. Fig. 10 compares the critical delays of some of the standard cells with uniform and tapered nanowires with varying amount of gate oxide thickness. As expected, cells with varying device geometry are slower than cells with uniform devices. While with increasing width, transistor performance increases, the OFF current also increases; to ensure good ratio, the doping concentration at the bottom was lowered than at the top. The performance degradation is mainly due to the higher threshold voltage of 22nm devices in the middle, which had the same doping as the bottom 32nm devices to minimize doping complexity in taper geometry. Table 1. shows the normalized power savings of standard cells with tapered geometry. The lower on-current in the tapered transistors are responsible for lower power consumption at the cost of delay. The overall density of the fabric increased by 17%, as the nanowire pitch needed to increase to maintain enough space at the bottom of the nanowires.

### 8. Conclusion

We proposed a wafer-scale manufacturing process flow for fine-grained vertical 3D-CMOS technology using existing industry foundry processes. Using process

emulations, we generated 3D models of various fabric components and combined them to create 3D standard cells. We performed electrical characterization of resultant 3D structures using process and device simulations. The device characteristics were used to extract compact model and together with interconnect parasitics, physical HSPICE netlists were created for circuit-level validation of 3D standard cells. Our bottom-up evaluation results prove the validity of our proposed flow paving the way for widespread adoption of 3D-IC technology.

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