Integrated Nanosystems with Junctionless Crossed Nanowire Transistors

Pritish Narayanan, Pavan Panchapakeshan, Jorge Kina, Chi On Chui and Csaba Andras Moritz

***Abstract*— Junctionless field-effect transistors (FETs) are promising emerging devices with simple doping profiles. In these devices, the channel is uniformly doped without the need for extremely good lateral doping abruptness or high thermal budget at source/channel and drain/channel junctions. This implies that device customization requirements are simplified compared to conventional enhancement-mode FETs. However, junctionless FETs have been discussed exclusively in the context of MOSFET replacement assuming other CMOS manufacturing, circuit and interconnect paradigms to be preserved intact.**

In this paper we argue for integration of junctionless devices into emerging nanofabrics. We propose junctionless crossed-nanowire FETs (xnwFETs) as the active devices for the Nanoscale Application Specific Integrated Circuits (NASICs) crossed nanowire fabric. We show that in addition to reducing customization requirements for individual nanodevices, the simpler device doping profile enables a scalable manufacturing pathway for NASICs where alignment and overlay requirements are minimized. In this pathway, a uniform 2-D nanowire grid may be assembled using unconventional or self-assembly based approaches without any overlay constraints. Overlay requirements exist only for subsequent photolithography steps, which is expected to be very precise ($3\sigma = \pm 3.3nm$ for 16nm technology node).

***Index Terms*— NASIC, Junctionless FET, crossed nanowire field effect transistors, manufacturing, CMOS replacement, nanofabrics**

I. Introduction

Emerging nanomaterials such as semiconductor nanowires [1], [2], carbon nanotubes [3], [4], graphene [5] etc. have been suggested as alternatives to conventional CMOS technology. However, research has largely concentrated on nanoelectronic devices, and paradigms for integration employing scalable manufacturing pathways have not been extensively explored.

At the nanoscale, it would be desirable to minimize customization requirements on devices and layouts (e.g. eliminating arbitrary sizing and placement of devices and arbitrary routing between them) by moving towards simple device structures and regular layouts such as parallel arrays and grids that are more easily realizable with unconventional and self-assembly based manufacturing approaches. Furthermore, instead of assuming arbitrary interconnection of devices, manufacturing would be simplified if both devices and interconnect could be formed as part of these regular layouts.

One nanoscale computing fabric incorporating such fabric-centric principles is Nanoscale Application Specific Integrated Circuits (NASICs) [6], [7], [8], [9]. NASICs are built on regular 2-D semiconductor nanowire grids with crossed nanowire field effect transistors (xnwFETs) at certain cross-points. NASICs typically use $n-$type xnwFETs and require a positive threshold voltage for correct cascading, noise and functionality [10]. Typically, $n+/p/n+$ drain/channel/source structures with an $n+$ gate were used with underlap for enhancement-mode behavior with positive V_{TH}. However, it would be desirable to simplify device engineering effort while still meeting circuit requirements.

One promising device that has made significant advances in recent research is the junctionless transistor or gated resistor [11], [12]. This device does not have drain/channel and source/channel junctions with sharp concentration gradients. Instead, the drain/source/channel regions are all uniformly doped $n+$ which makes for simpler manufacturing. The gate-channel workfunction difference is used to deplete the channel of carriers, switching off the device. The key insight is that this is possible at the nanoscale due to the ultra-small channel cross-section.

Junctionless FETs proposed in prior work have been targeted as CMOS replacement devices with the assumption that CMOS circuit styles and paradigms for interconnection will be preserved intact. However, the operating principles of junctionless devices may be applied to nanofabrics as well. In this paper, we propose junctionless xnwFETs for NASICs. We simulate the I-V characteristics of these structures through detailed physics-based 3-D simulations. We verify that the devices meet circuit requirements for correct cascading and noise, thereby enabling their integration into the fabric. We discuss manufacturing implications and show that the simpler structure of junctionless xnwFETs, in addition to reducing device-level customization requirements, also mitigates overlay and alignment requirements for the fabric as a whole, thereby simplifying the NASIC manufacturing pathway.

The rest of the paper is organized as follows: Section II provides a brief overview of NASICs. Section III introduces the junctionless crossed-nanowire FET and discusses its electrical characteristics. Section IV discusses the manufacturing implications of using junctionless xnwFETs in the NASIC fabric in detail. Section V concludes the paper.

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P. Narayanan, P. Panchapakeshan and C. A. Moritz are with the Dept. of Electrical and Computer Engineering, University of Massachusetts, Amherst MA 01003. andras@ecs.umass.edu

J. Kina and C. O. Chui are with the Dept. of Electrical Engineering, University of California Los Angeles, CA.

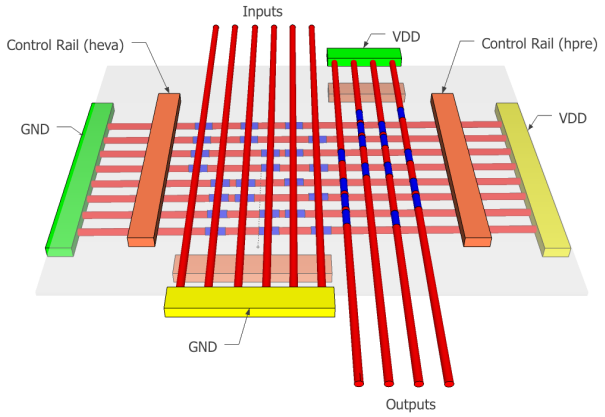

Fig. 1. 1-bit NASIC adder with $n-$type enhancement-mode xnwFETs. $p-$type channels (blue) are created on both vertical and horizontal nanowires with $n+$ source/drain regions for E-mode behavior.

II. NASICs Overview

The NASIC fabric is built on 2-D semiconductor nanowire grids with crossed nanowire field-effect transistors (xnwFETs) at certain crosspoints. The channel of a xnwFET is aligned along one NW while the perpendicular NW acts as gate. Fig. 1 shows a 1-bit full adder implemented on the NASIC fabric with enhancement mode xnwFETs. This includes a semiconductor nanowire grid with peripheral microwires (MW) that carry V_{DD}, V_{SS} and dynamic control signals. E-mode xnwFETs are shown at certain crosspoints in the diagram. p channels of xnwFETs (blue regions) are oriented horizontally on the left plane, and vertically on the right. Inputs are received from vertical nanowires in the left plane. These act as $n+$ gates to horizontal nanowire FETs implementing one stage of a dynamic circuit. The output of horizontal nanowires acts as $n+$ gate to the next set of transistors whose channels are aligned in the vertical direction (right NAND plane). Multiple such NASIC tiles are cascaded together to form more complex circuitry such as microprocessors [14] and image processing systems [15].

III. Junctionless Crossed Nanowire Field Effect Transistors

Fig. 2(a) shows one possible enhancement-mode xnwFET structure integrated into NASICs. In this structure, the channel region is doped $p-$type and the gate/source/drain are all doped $n+$. As discussed previously, the enhancement mode device operates on the principle of channel inversion, with a sufficiently high positive bias on the gate inducing an $n-$type conducting channel between the $n+$ doped source and drain regions. An optional underlap or substrate bias may be applied to enhancement-mode xnwFETs to tune the I-V characteristics and modulate device parameters such as the threshold voltage and on/off current ratios [10], [9], [13].

Fig. 2(b) shows the proposed junctionless xnwFET device, similar to [11], [12]. In this device, the bottom nanowire does not have any sharp concentration gradients, or junctions between p channels and $n+$ source/drain regions. Instead, the doping profile along the length of the bottom nanowire

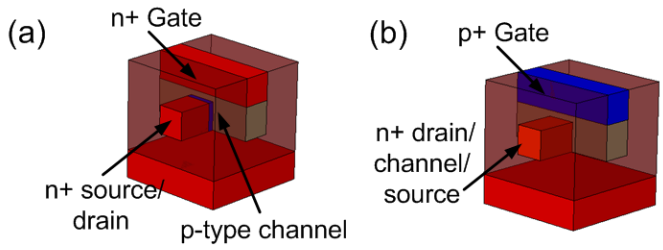

Fig. 2. (a) Enhancement-mode devices with channel inversion, and (b) Junctionless $n-$type device with $p+$ gate

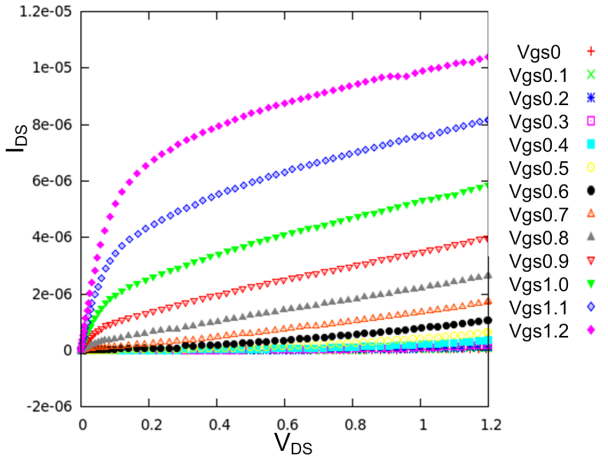

Fig. 3. I-V characteristics for junctionless device

is uniform (in this case $n+$). The workfunction difference between the $p+$ gate and the $n+$ channel depletes the majority carriers and prevents conduction through the channel at zero bias. However, as a positive bias is applied to the gate, majority carriers are induced in the channel leading to conduction.

Accurate 3-D physics-based simulations of the junctionless structures were carried out using Synopsys Sentaurus to extract device behavior. Channel and gate widths were assumed to be 10nm[1]. HfO_2 was used as high-k gate dielectric material with a thickness of 2nm. The gate is doped at $8 \times 10^{19} dopants/cm^3$ and the channel is doped $4 \times 10^{19} dopants/cm^3$. A substrate bias of -3V is employed to aid in channel depletion and provide a higher positive threshold voltage. Table I summarizes all simulation parameters.

Currents in the channel were simulated for varying values of V_{GS} and V_{DS} and threshold voltage, on/off current ratios were extracted. Fig. 3 shows the I-V characteristics of the $n-$type junctionless FET. Simulations show a positive V_{TH} of 0.52 V and on/off current ratio $> 10^3$, which meet the requirements for correct cascading and adequate noise margins for NASIC circuit styles [10]. It must be noted that this work shows one possible junctionless xnwFET; other

[1]While a larger gate could provide better electrostatic control this assumption is incompatible with NASICs. NASICs is a nanowire grid based fabric, with channels of one stage directly becoming gates to the next stage along the length of a nanowire

TABLE I
DEVICE SIMULATION PARAMETERS

Parameter	Value
Channel width	10nm
Gate width	10nm
Gate oxide thickness	2nm
Bottom oxide	10nm
Channel doping	$4 \times 10^{19} dopants/cm^3$
Gate doping	$8 \times 10^{19} dopants/cm^3$
Substrate Bias	-3V

structures using cylindrical nanowires, omega gates etc., and further optimization of devices for better performance will be explored as part of future work.

IV. MANUFACTURING IMPLICATIONS

A scalable manufacturing pathway for the NASIC fabric, including simultaneous creation of enhancement-mode xnwFETs and interconnect was described in [16]. This manufacturing pathway used a combination of self-assembly (for scalable assembly of nanostructures) in conjunction with lithography (for contacts, control and logic). It was shown that fabric choices reduced manufacturing requirements down to two key issues: assembly of parallel nanowire grids on to a substrate and defining the positions of xnwFET channels on the grid to achieve the desired logic functions. The latter step, called *functionalization*, is done lithographically. With enhancement mode devices, at least two separate functionalization steps are required for horizontal and vertical nanowires. This is because source/channel/drain profiles need to be created on both nanowire layers (see Fig. 1). Importantly, the two step functionalization has a requirement for alignment between the two layers, i.e. vertical gate nanowires would need to align against predefined channel regions on the horizontal nanowires.

Using junctionless xnwFETs, in addition to mitigating customization requirements for individual devices, alleviates functionalization requirements. Specifically, since non-uniform doping profiles are not needed on the channel nanowires, a uniform nanowire grid with horizontal and vertical nanowires can be assembled before any customization, implying that there is no alignment requirement for the nanowire grid itself. The only requirement for assembly of this grid would be acheiving one nanowire per pitch in both directions. Furthermore, since there is no custom doping profile, the channels are automatically self-aligned at the cross-points of the nanowire grid, since gate-induced channel depletion is achieved locally. After the grid has been assembled, all lithographic functionalization could be carried out, which implies that alignment requirements exist only between successive lithographic masks. This overlay alignment for conventional lithography is very precise (ITRS 2009 projects a $3\sigma = \pm 3.3nm$ overlay precision for 16nm CMOS [17]).

Fig. 4(a) shows the nanowire grid assembled *a priori* to any functionalization, with no alignment requirement. Horizontal wires are $n+$ and vertical wires are $p+$. On the left plane n-type xnwFETs are implemented with $p+$ gate and $n+$ channel. Similarly, on the right plane, the $n+$ horizontal nanowires are gates for $p+$ channels. Since at this stage all crosspoints are transistors, a *defunctionalization* step is needed. Defunctionalization is done using a lithographic mask (Fig. 4(b)) to remove FET characteristics at certain crosspoints and simultaneously define devices and interconnect. This processing step uses a nickel silicide metallization step similar to [18]. Briefly, Nickel is deposited and a thermal annealing step is done. This causes Nickel to diffuse into the Silicon nanowires and forms Nickel Silicide which has metallic properties (Fig. 4(c)).

The defunctionalization mechanism has a different impact on the left and right stages. The novelty of the approach lies in the fact that on the left plane, the gate is silicided (eliminating the workfunction difference between the perpendicular nanowires and 'erasing' the FET), whereas on the right plane, the channel is silicided, resulting in a low resistance conducting path without any gate modulation.

The ability to defunctionalize crosspoints in both planes simultaneously in conjunction with the device property that the depletion region is always self-aligned to the crosspoint implies that alignment requirements are alleviated; as opposed to the enhancement mode case, nanowires need not be aligned correctly against pre-functionalized channels. A nanowire could be laterally shifted from its nominal position and remain self-aligned. Furthermore, the elimination of a lithography mask would imply a higher overlay-limited yield. Contacts, power and control rails etc. can subsequently be created to define interfaces to the microscale (Fig. 4(d)).

This approach is easily extendible to a large scale design, with a large nanowire grid that can be 'sliced' after assembly into individual tiles using an etch-back process. An example with two tiles and etch-back is shown in Fig. 5. In this figure, two NASIC tiles are created from an initial uniform nanowire grid. Silicidation is done across the entire design to define positions of all junctionless xnwFETs. Disconnections are then made using an etch process to disconnect nanowires at certain locations and demarcate tiles (Fig. 5(c) and (d)). Given that the underlying pattern of nanowires is uniform (grid structure), the first lithographic mask may be offset with tolerance and without loss of yield.

V. CONCLUSIONS

Junctionless crossed-nanowire field effect transistors for the NASIC fabric were proposed and shown to meet NASIC circuit requirements including positive threshold voltage and on/off current ratios. Implications of junctionless xnwFETs for the NASIC manufacturing pathway were discussed. A new 'grid-first' manufacturing sequence is demostrated where all lithographic functionalization is carried out after assembly of the nanowire grid. Defunctionalization of crosspoints using a Nickel silicide-based metallization process was discussed, mitigating alignment requirements and eliminating a lithographic mask.

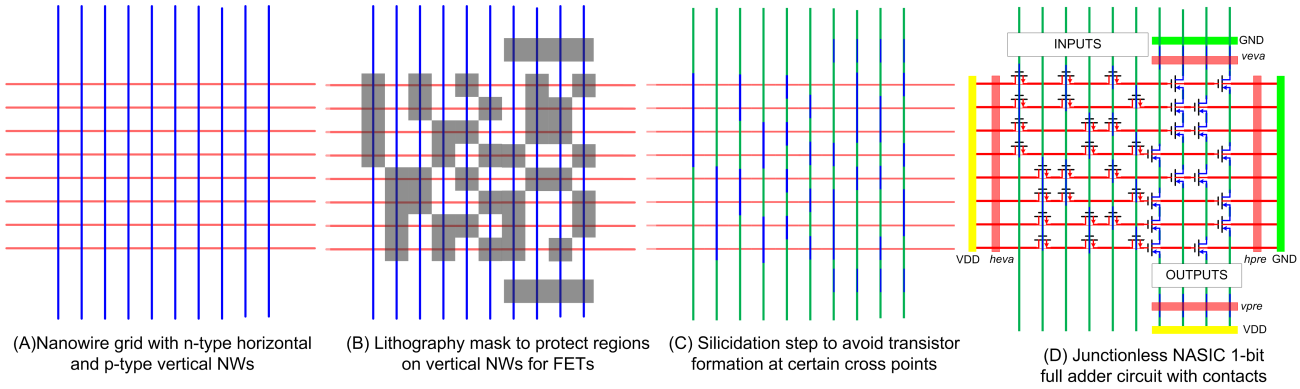

Fig. 4. NASIC manufacturing pathway with Junctionless xnwFETs and 'grid-first' assembly.

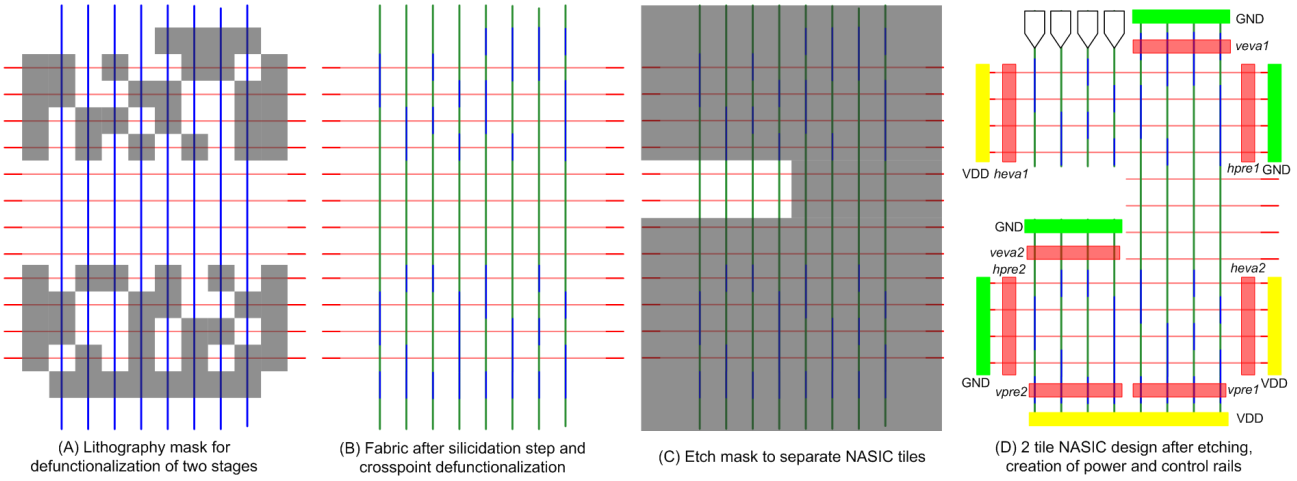

Fig. 5. Scalable manufacturing pathway shown for two tile design with nanowire etch-back process: this pathway is easily extendible to large-scale NASIC designs with multiple interacting tiles

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