3-D Integration Requirements for Hybrid Nanoscale-CMOS Fabrics

Pavan Panchapakeshan, Priyamvada Vijayakumar, Pritish Narayanan, Chi On Chui, Israel Koren and Csaba Andras Moritz

***Abstract* — Several nanoscale-computing fabrics based on novel materials such as semiconductor nanowires, carbon nanotubes, graphene, etc. have been proposed in recent years. However, their integration and interfacing with external CMOS has received only limited attention. In this paper we explore integration challenges for nanoscale fabrics focusing on registration and overlay requirements especially. We address the following questions: (i) How can we mitigate the overlay requirements between nano-manufacturing and conventional lithography steps? (ii) How much overlay precision is necessary between process steps? and (iii) What is the impact on yield if different overlays are used?**

We propose and evaluate a new 3D integration approach that combines standard CMOS design rules with nano-manufacturing constraints. For a nanoprocessor design implemented in N^3ASIC (a hybrid nanowire-CMOS fabric) we show that a 100% yield is achievable even for overlay precisions achievable with current CMOS manufacturing ($3\sigma=\pm8$nm, ITRS 2009) while still retaining 3X density advantage compared to a projected 16nm CMOS scaled design.

Index Terms – 3-D integration, mask overlay, alignment, nanofabrics, N^3ASICs, NASIC, nanowires, nanoscale computing

I. Introduction

Manufacturing of integrated nanosystems with scalable assembly of sub-lithographic nanostructures continues to pose significant challenges. While unconventional manufacturing techniques such as imprint lithography [1] and SNAP [2] can produce ultra-dense regular structures at sub-10nm features, alignment with respect to previously formed patterns is still a concern (e.g., the overlay alignment for imprint lithography is very poor at $3\sigma = \pm105$nm [3]). Photolithography on the other hand has excellent mask overlay precision but may not achieve the same density overall (since individual layers may be benefitting from using nanoscale manufacturing techniques).

In this paper we propose a hybrid nano-CMOS 3-D integration approach that combines the advantages of unconventional and conventional manufacturing processes. We discuss the overlay requirements for hybrid nanofabrics, and demonstrate how full 3-D integration may be achieved using standard CMOS design rules. We show that design choices and order of process can mitigate overlay and alignment requirements, while retaining density benefits of sub-lithographic processes.

We estimate the yield for different overlay precisions (as projected by ITRS 2009 [4]) for the proposed approach. We present a 3-D nanofabric called N^3ASICs, that can be built using the proposed approach and evaluate its benefits against 16nm CMOS technology. A nanoprocessor (WISP-0 [5]) is mapped to this fabric for the purpose of study. Results show that a yield of 100% is obtained even for an overlay imprecision of 8nm (based on manufacturing solutions known according to ITRS 2009) with a density advantage of 3X.

The key contributions of the paper are (i) a 3-D integrated approach to build nano-CMOS hybrid systems is presented; (ii) the dependence of overlay-limited yield on the order of manufacturing process is discussed; and (iii) yield implications for different overlay precisions are evaluated.

The rest of the paper is organized as follows: Section II describes 3-D integration requirements and approaches for nanosystems, Section III presents a discussion on alignment and overlay requirements, Section IV describes the simulation methodology for overlay limited yield and results obtained, and Section V concludes the paper.

II. 3-D Integration Requirements

Nanofabrication techniques based on contact patterning or self-assembly based approaches favor the formation of regular periodic structures such as grids. Registration requirements in such regular structures are alleviated since an initial lithography mask may be 'offset' with no loss of functionality. For example, NASICs [6][7][8][9][10][11] is a 2-D nanowire grid based fabric which uses lithography masks for functionalization, contacts etc. A detailed study of the implications of mask overlay and misalignment was carried out for NASICs in [12]. It was observed that a yield of ~70% can be obtained for an overlay of $3\sigma = \pm5.7$nm (manufacturing solutions known, ITRS 2009 [4]). In this paper, we discuss how regular nanofabrics could be built with full 3-D CMOS integration, while further mitigating overlay requirements and carefully addressing density implications.

One approach to build a fully integrated 3-D fabric is to use only optical lithography for all the process steps. The

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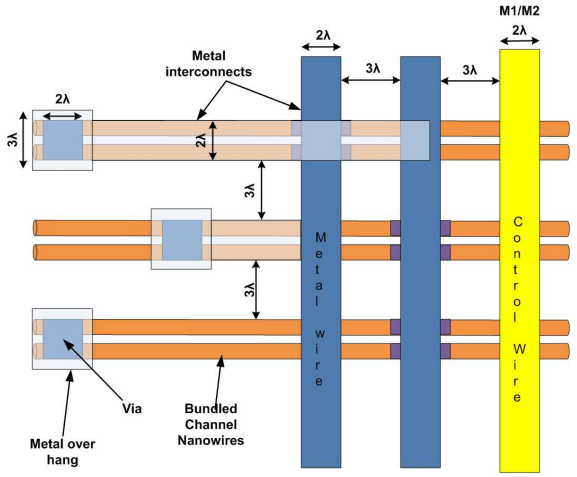

Figure 1 NW design rules for 3-D integration

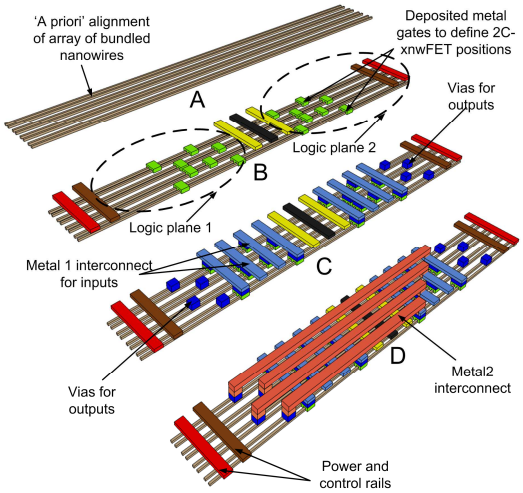

Figure 3 A simplified manufacturing sequence

extremely good overlay precision of CMOS can be exploited with this approach. Therefore, yield obtained will be comparable to CMOS process yield. However, the approach is expected to have low density when compared to techniques that use self-assembly/unconventional nanofabrication techniques since it is limited by optical lithography.

A second approach would be to use unconventional approaches on top of a conventional manufacturing flow to obtain a 3D integrated fabric of high density. Such an approach has been examined in CMOL [13] and FPNI [14] nanofabrics, where unconventional techniques such as nanoimprint are necessary after the fabrication of CMOS layers. As mentioned previously, overlay alignment precision needed for imprint lithography is $3\sigma=\pm 105$nm [3], which implies significant challenges in alignment against previously defined lithographic features. Such a large overlay misalignment can contribute to significant yield loss (or conversely trading-off much of the density benefit using well separated features for acceptable yield) and is not ideal.

Our current work lays emphasis on the importance of the manufacturing sequence when unconventional and conventional manufacturing techniques are employed in conjunction. We propose a nano-CMOS integration approach, which considers the *order of manufacturing process steps* along with fabric design choices; these aid in mitigating mask overlay while still achieving an ultra dense fabric.

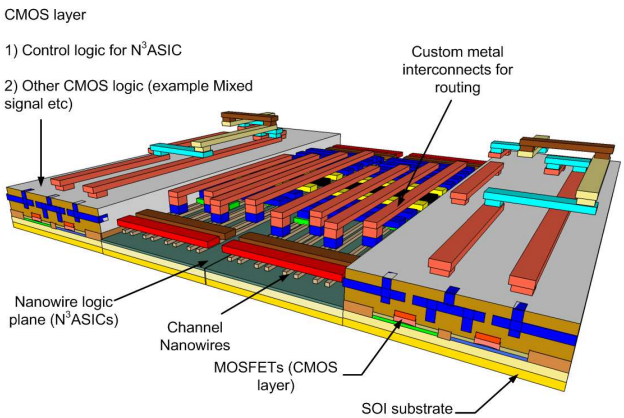

Figure 2 A Nano-CMOS 3-D integrated fabric

In this approach a single unconventional manufacturing is carried out *a priori* to all lithography steps to define high-density nanostructures. This overcomes the overlay challenge for nano-manufacturing, since the first step of the manufacturing sequence would not have any overlay requirement. Furthermore if the defined nanostructure pattern is regular (e.g. parallel arrays), the first lithographic mask has overlay tolerance, i.e. it may be 'offset' over the array without yield loss. All subsequent steps could be lithographic with excellent overlay precision. This approach achieves 3-D integration without any special manufacturing requirements while ensuring finer nanoscale resolution (and consequently higher density) than can be achieved with lithography at the bottom (where the logic density is improved).

To enable direct integration into a conventional lithography flow, CMOS design rules (Fig. 1) are followed for all subsequent steps such as creation of metal vias, interconnect, contact rails etc. Fig. 1 shows the design rules across nanoscale features and lithographic scale length λ. Width and spacing of the bottom nanowire grid must adhere to CMOS design rules. The CMOS design rules for 16nm were as projected by ITRS and [15]. Metal 1 pitch and via spacing determine the spacing between the nanowire bundles. This is projected to be 40nm for 16nm technology node.

A fabric incorporating these principles of 3-D integration is Nanoscale 3-D Application Specific Integrated Circuits (N^3ASICs) [16] (Fig. 2). The fabric can be built on a single ultra-thin SOI wafer, with a direct-patterned nanowire logic plane surrounded by support CMOS circuitry (e.g. for external control). Lithographically defined vias or area-distributed interfaces connect the nanowire arrays through a CMOS metal stack. Detailed N^3ASIC description and evaluations can be found in [16].

The step-by-step 3-D integration approach for N^3ASICs is shown in Fig. 3. Nanowires may be direct-patterned on Silicon-on-Insulator substrates (Fig. 3A) through

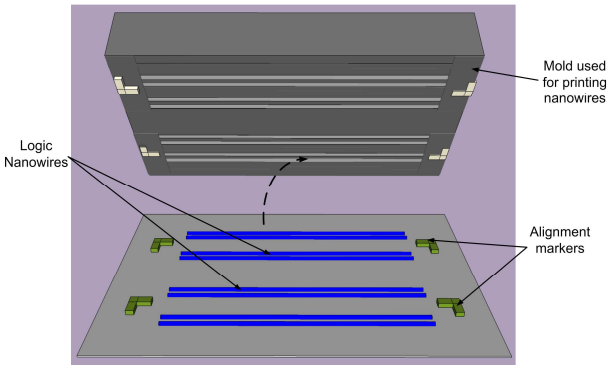

Figure 4 Nanowires and the alignment markers in the same mold for NIL technique

unconventional approaches such as SNAP and imprint lithography. Since metal vias are used to contact channel nanowires, the spacing of the channel nanowires is determined by design rules for via spacing. Since channel nanowires could have much smaller dimensions than metal vias, they are bundled into pairs to make better contact, and provide for dual channel crossed-nanowire field-effect transistors (2C-xnwFETs) [16].

Following the *a priori* patterning of nanowire layers, lithography is used for contact creation and metal gate deposition. This step defines the positions of logic planes and transistors on the grid to achieve the required functionality (Fig. 3B). A self-aligning ion implantation is then used to create n+/p/n+ regions. Finally, metal stacks implement interconnects similar to traditional CMOS. Metal 1 is used to connect inputs as shown in Fig. 3C. Metal 2 is used to connect two different logic planes as depicted by Fig. 3D. Area-distributed standard pins or vias are used to connect inputs and outputs of the nanowire logic planes to the CMOS routing stack. Metal interconnects and vias help in achieving arbitrary routing.

N^3ASICs is found to be 3X denser than CMOS for a processor design. The density advantage of N^3ASICs is due to the dense nanowire array at the bottom (implying the use of devices with smaller dimensions when compared to conventional CMOS FETs), use of single type FET to realize logic, implicit latching on the nanowires (which ensures that there is no need for area expensive latches and flip-flops) and finally reduced transistor count compared to CMOS.

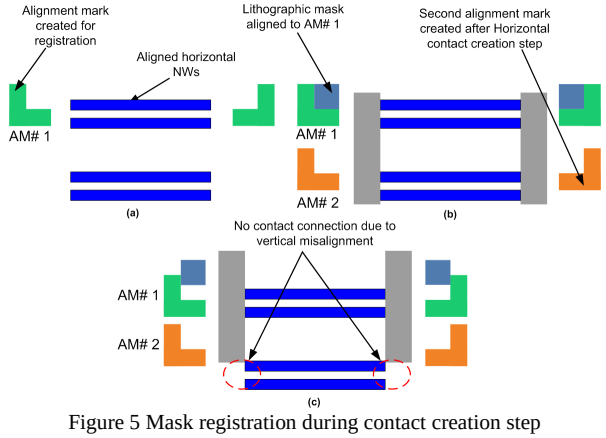

Figure 5 Mask registration during contact creation step

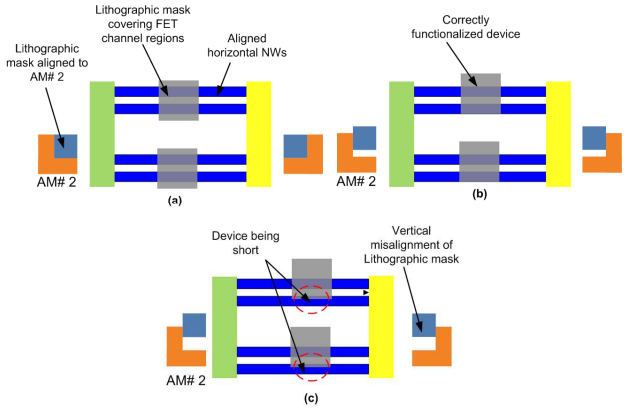

Figure 6 Mask registration during functionalization step

Since the nanowire layer confirms to CMOS design rules, the spacing between the nanowires is greater compared to a 2-D grid based NASIC fabric. While the NASIC fabric is 33X denser [6] than functionally equivalent CMOS WISP-0 design, the use of design rules, while alleviating manufacturing requirements, reduces the density advantage of N^3ASICs to 3X.

III. Alignment and Mask Overlay

Nanowire patterning may be carried out using NIL [1] or SNAP [2]. As mentioned, this step is carried out prior to any lithographic step and hence has no overlay requirement. In addition, alignment markers can be created for registration of photolithographic steps at the same time as the logic nanowires. If NIL is used, alignment markers for subsequent lithography steps and logic nanowires can be part of the same mold and hence transferred to the substrate in a self-aligned fashion as shown in Fig. 4. In the case of SNAP, where an arbitrary alignment marker may be difficult to achieve, patterned nanowires of different dimensions can be used as Moire patterns/fringes [17].

Since the underlying pattern of nanowires is uniform, this allows the first lithographic mask to be horizontally offset with some tolerance and still achieve correct functionality. Fig. 5 demonstrates the mask registration process during contact creation step. Fig. 5(a) shows the nanowires and the alignment markers created using technique like NIL. Fig. 5(b) shows the first lithographic step. Alignment marker (AM# 1) 1 is used as the alignment target and the mask is perfectly aligned in this scenario. New alignment markers (AM# 2) are created during the contact step which is used for aligning subsequent mask. Fig. 5(c) shows an excessive misalignment case which results in nanowires being not contacted by the power rails resulting in a defective chip.

Fig. 6 shows the defects that are caused due to the mask misalignment during functionalization to create metal gates and 2C-xnwFETs [18]. A large vertical misalignment leads to an incorrectly shorted device, impacting the yield. Also, this step has little tolerance to horizontal misalignment as contacts have already been defined. Fig. 6(b) shows correctly functionalized devices despite some overlay misalignment (demonstrating the misalignment tolerance in

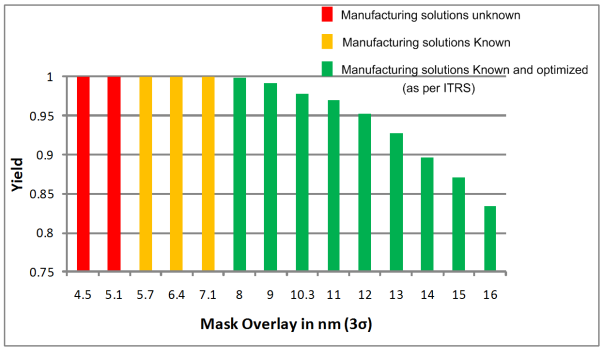

Figure 7 Yield vs. Overlay for 3D integrated fabric

this step). Fig. 6(c) shows shorted devices due to excessive overlay misalignment. Additional alignment markers (not shown in Fig. 6) will be created during this step which will be the alignment targets for the subsequent step.

IV. Overlay Simulation Results

The WISP-0 [5][6] nanoscale processor design was mapped onto the N^{3}ASIC fabric. Overlay misalignment between successive masks were modelled as Gaussian random variables, and Monte Carlo simulations were carried out in a custom simulator to determine the number of functioning chips. The simulations were carried out for several 3σ overlay misalignment values projected by ITRS 2009 [4].

The manufacturing of 3D integrated fabric employs usage of large number of masks. The contact creation and metal gate deposition steps are the most critical to mask overlay (since they involve alignment to the smallest features) and contribute significantly to the yield loss. Yield loss due to mask overlay during metal stack creation is minimal (identical to conventional CMOS). Hence metal stacks higher than M2 layer have not been considered in these simulations.

The results in Fig. 7 show that close to 99% yield may be obtained for 3σ=±9nm overlay (manufacturing solutions known as per ITRS 2009) when constructing a uniform nanowire bundle with λ=8nm (16nm technology node) in the 3D integrated fabric. Within a bundle the width of nanowires is 5nm each, with 6nm spacing to accommodate 16nm vias. Fig. 7 shows that even with a pessimistic mask overlay projection of 3σ=±16nm a yield of 83% can be observed. These overlay requirements are far less stringent than the requirement for 16nm CMOS (3σ=±3.3nm for 16nm CMOS, per ITRS 2009).

It is evident from the results that the use of regular structure (like the nanowire arrays in N^{3}ASICs) does not impose stringent constraints on overlay precision requirement. Further, fewer masks are required to manufacture this fabric which is beneficial from both yield and cost perspective.

The simulation methodology employed enables addressing key overlay and registration requirements. It is possible to estimate the overlay-limited yield for a range of overlay projections. It is also possible to address sensitivity of the overlay-limited yield to key fabric parameters such as the width and pitch of nanowires.

V. Conclusion

We present a 3-D integration and fabric approach. By analyzing the available design choices and careful consideration of the order of manufacturing processes, the impact of mask overlay is mitigated. The N^{3}ASIC 3-D nanofabric, built using these principles, consists of a regular dense nanowire array at the bottom, followed by CMOS interconnect layers on the top is 3X denser than CMOS and is realizable with available manufacturing techniques at very minimal yield loss. Assuming an overlay precision of 9nm or better results in a yield of 100%. In contrast, irregular structures would have more stringent mask overlay requirements. For example, the proposed approach also has considerably greater tolerance (~3X) to overlay imprecision than 16nm CMOS that requires a 3nm precision at 16nm node as per ITRS 2009.

References

[1] T. Mårtensson, P. Carlberg, M. Borgström, L. Montelius, W. Seifert, and L. Samuelson, "Nanowire Arrays Defined by Nanoimprint Lithography," *Nano Letters*, vol. 4, no. 4, pp. 699-702, Apr. 2004.

[2] D. Wang, Y. Bunimovich, A. Boukai, and J. R. Heath, "Two-dimensional single-crystal nanowire arrays," Dec-2007. [Online]. Available: http://www.nanoarchive.org/1853/.

[3] C. Picciotto, J. Gao, Z. Yu, and W. Wu, "Alignment for imprint lithography using nDSE and shallow molds," *Nanotechnology*, vol. 20, no. 25, p. 255304, Jun. 2009.

[4] "2009 ITRS http://www.itrs.net/Links/2009ITRS/Home2009.html."

[5] T. Wang, M. Ben-naser, Y. Guo, and C. A. Moritz, "Wire-streaming processors on 2-D nanowire fabrics," *IN NANOTECH 2005. NANO SCIENCE AND TECHNOLOGY INSTITUTE*, 2005.

[6] C. A. Moritz, P. Narayanan, and C. O. Chui, "Nanoscale Application-Specific Integrated Circuits," in *Nanoelectronic Circuit Design*, N. K. Jha and D. Chen, Eds. Springer New York, 2011, pp. 215-275.

[7] P. Narayanan, M. Leuchtenburg, T. Wang, and C. A. Moritz, "CMOS Control Enabled Single-Type FET NASIC," in *2008 IEEE Computer Society Annual Symposium on VLSI*, Montpellier, France, 2008, pp. 191-196.

[8] T. Wang, P. Narayanan, and C. Andras Moritz, "Heterogeneous Two-Level Logic and Its Density and Fault Tolerance Implications in Nanoscale Fabrics," *IEEE Transactions on Nanotechnology*, vol. 8, no. 1, pp. 22-30, Jan. 2009.

[9] C. A. Moritz et al., "Fault-Tolerant Nanoscale Processors on Semiconductor Nanowire Grids," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 11, pp. 2422-2437, Nov. 2007.

[10] T. Wang, P. Narayanan, and C. A. Moritz, "Combining 2-level logic families in grid-based nanoscale fabrics," in *2007 IEEE International Symposium on Nanoscale Architectures*, San Jose, CA, USA, 2007, pp. 101-108.

[11] P. Narayanan, C. A. Moritz, K. W. Park, and C. O. Chui, "Validating cascading of crossbar circuits with an integrated device-circuit exploration," in *2009 IEEE/ACM International Symposium on Nanoscale Architectures*, San Francisco, CA, USA, 2009, pp. 37-42.

[12] P. Vijayakumar, P. Narayanan, I. Koren, C. M. Krishna, and C. A. Moritz, "Impact of Nanomanufacturing Flow on Systematic Yield Losses in Nanoscale Fabrics," in *2011 IEEE/ACM International Symposium on Nanoscale Architectures*, 2011.

[13] X. Ma, D. B. Strukov, J. H. Lee, and K. K. Likharev, "Afterlife for silicon: CMOL circuit architectures," in *Nanotechnology, 2005. 5th IEEE Conference on*, 2005, pp. 175-178 vol. 1.

[14] G. S. Snider and R. S. Williams, “Nano/CMOS architectures using a field-programmable nanowire interconnect,” *Nanotechnology*, vol. 18, no. 3, p. 035204, Jan. 2007.

[15] C. Bencher, H. Dai, and Y. Chen, “Gridded design rule scaling: taking the CPU toward the 16nm node,” in *Proceedings of SPIE*, San Jose, CA, USA, 2009, p. 72740G-72740G-10.

[16] P. Panchapakeshan, P. Narayanan, and C. A. Moritz, “N^3ASICs: Designing Nanofabrics with Fine-Grained CMOS Integration,” in *2011 IEEE/ACM International Symposium on Nanoscale Architectures*, 2011.

[17] S. H. Zaidi, “Moire interferometric alignment and overlay techniques,” in *Proceedings of SPIE*, San Jose, CA, USA, 1994, pp. 371-382.

[18] P. Narayanan, K. W. Park, C. O. Chui, and C. A. Moritz, “Manufacturing pathway and associated challenges for nanoscale computational systems,” in *Nanotechnology, 2009. IEEE-NANO 2009. 9th IEEE Conference on*, 2009, pp. 119 -122.