Experimental Prototyping of beyond-CMOS Nanowire Computing Fabrics

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***Abstract*— Nanoscale 3D-integrated Application Specific ICs (N^3ASICs) [1], a computing fabric based on semiconductor nanowire grids, is targeted as a scalable alternative to end-of-the-line CMOS. In contrast to device-centric approaches like CMOS, N^3ASIC design choices across device, circuit and architecture levels are geared towards reducing manufacturing requirements while focusing on overall benefits. In this fabric, regular arrays with limited customization imply mitigated overlay precision requirements, novel circuit styles with single-type cross-nanowire FETs eliminate the need for arbitrary fine-grain sizing, doping and routing. In addition, junctionless transistors eliminate the need for stringent control of doping profiles. In this paper, we present theoretical and experimental progress towards realizing a functional N^3ASIC prototype with junctionless transistors as active cross-point devices. We first validate this device concept through detailed 3D device simulations. We then present a manufacturing pathway as well as show experimental results demonstrating a proof-of-concept metal-gated junctionless nanowire device and N^3ASIC tile structure with sub-30nm nanowires.**

***Index Terms*—N^3ASICs, Semiconductor Nanowires, Nanoscale Computing Fabrics, Nanofabrication, E-Beam Lithography, Manufacturing Pathway**

I. Introduction

CMOS scaling into the sub-20nm regime is becoming increasingly challenging due to complex manufacturing requirements. CMOS requires doping and sizing of transistors at nanoscale precision along with arbitrary placement for custom layouts. According to ITRS the overlay precision requirements for 16nm CMOS would be ±3nm [2], a precision for which manufacturing solutions are as yet unknown. To mitigate manufacturing challenges and to maintain technology scaling benefits at nanoscale, while maximizing system level benefits, we proposed a novel computing fabric called Nanoscale 3D Application Specific Integrated Circuits (N^3ASIC) [1]. N^3ASIC relaxes manufacturing requirements through simplified regular grid-based layouts without arbitrary placement and routing, and uses single-type, uniformly sized transistors. Benchmarking results at 16nm for a processor design show N^3ASICs to be up to 3x denser and 5x more power efficient than an equivalent CMOS design [1]. Benchmarking results for N^3ASIC volatile memory shows 2x performance and 35x leakage power benefits, when compared to CMOS SRAM at 16nm [3][4]. In addition, due to N^3ASICs regular physical layout and choices at all levels of abstraction, the overlay alignment requirements are significantly less than in CMOS. Our yield simulation results show 100% yield can be achieved with relaxed overlay of ±8nm for N^3ASIC fabric implementation at 16nm technology node [5]. The process technology for such precision is known today and is in use.

In this paper, we present theoretical and experimental progress towards realizing a functional N^3ASIC prototype. We first show how the manufacturing requirements of N^3ASIC can be further simplified by using junctionless nanowire transistors as active cross-point devices. In junctionless transistors, the source, channel and drain are all uniformly doped without the need for abrupt doping profiles. The workfunction difference between the metal gate and channel is used to control gate depletion/accumulation.

We explore integration aspects of junctionless nanowire transistors into the N^3ASIC fabric. Through detailed 3D physics-based simulations of device structures we validate device behavior. We show that these junctionless transistors have the requisite threshold voltage and on/off ratio parameters for adequate noise margins and cascading of N^3ASICs logic and memory circuits. In order to take these concepts from theoretical studies and simulations to realization, we develop a detailed manufacturing pathway for N^3ASIC, and show recent progress towards building junctionless devices and an N^3ASICs experimental prototype.

We discuss our prototyping approach using Electron Beam Lithography, and show key results. This includes doped and direct patterned nanowires at sub-30nm dimensions on a Silicon-on-Insulator (SOI) substrate, characterized behavior of a normally-off metal-gate depleted junctionless transistor with three orders of magnitude on/off current ratios and a threshold voltage of ~ -0.3V, and a fabricated N^3ASIC crossbar structure built using the proposed manufacturing pathway.

The paper is organized as follows: In section II, we present an overview of the fabric and show its core components including the junctionless device; in section III, we present the detailed manufacturing pathway; in section IV, we highlight

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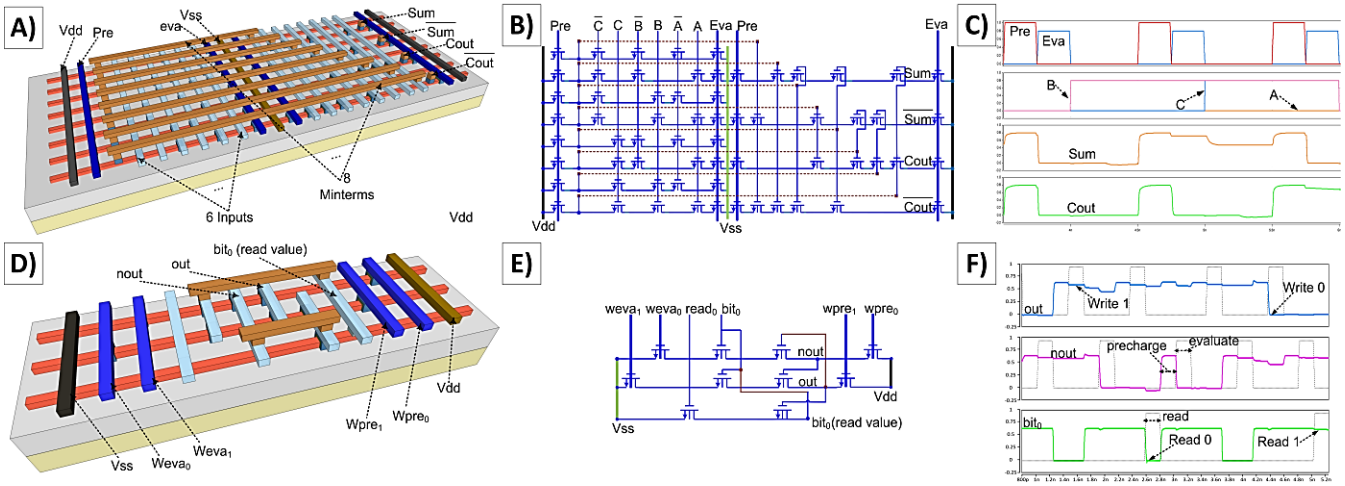


Fig.1 Logic and memory implementations in N^{3}ASIC fabric, A) Physical layout of full adder, B) Full adder circuit schematic with dynamic circuit style , C) Simulated waveforms showing adder functionality, D) volatile memory (10T-NWRAM) in N^{3}ASIC fabric. D) Schematic of 10T-NWRAM, E) Simulated waveforms showing read, write operations

key milestones in N^{3}ASIC experimental prototyping; in section V, we conclude the paper.

II. N^{3}ASIC FABRIC OVERVIEW

N^{3}ASIC is a physical fabric framework that enables manufacturing friendly integration of nanoscale devices and interconnects to achieve logic and memory functionalities. At the core of N^{3}ASIC fabric are arrays of semiconducting nanowires, which serve as building blocks; input signals are carried through orthogonal metal gates, and the location of transistors at certain cross-points together with the clocking control scheme determines the functionality being implemented. This organization of nanowire and metal gates in a grid like layout simplifies manufacturability considerably, since the pattern requirement is very regular with lines in two dimensions.

Dynamic circuit styles, amenable to implementation on these regular fabrics, are used. These circuit schemes use crossed-nanowire FET devices that are of a single doping-type and are identically sized [7][8][9], in contrast to CMOS circuits that require arbitrary sizing, doping and placement.

Fig. 1A shows a 1-bit full adder implementation on the N^{3}ASICs fabric; Fig. 1B shows the equivalent circuit schematic. This implementation uses a cascaded 2-level NAND-NAND logic style with dynamic circuits [1][7]. Inputs are received on vertical metal wires (M1) of the left tile; product-terms are generated at the outputs of this tile and through vias and M2 wires, are routed to the inputs of the second tile; carry and sum outputs of the adder are generated at the output vias of the second tile. These outputs may be cascaded to subsequent stages using the metal stack. HSPICE circuit simulations validate circuit functionality (Fig. 1C).

Fig. 1D and 1E show fabric and circuit schematics of a 10 Transistor Quasi-Static Nanowire RAM (10T - NWRAM) [4][3]. This circuit implements cross-coupled volatile memory without the need for complementary devices or careful sizing of FETs required in SRAM. True and complementary information bits are stored in cross-coupled dynamic NAND gates, and separate access signals are used for read/write. The 10T-NWRAM shares features of both static (cross-coupled) and dynamic (circuit style, restore) volatile memory, but with better performance than SRAM. HSPICE circuit simulations validating volatile memory behavior are shown in Fig. 1F.

Benchmarking results of N^{3}ASIC logic (a processor design, WISP-0 [1]) showed 3x density and 5x active power benefits against equivalent CMOS design at 16nm [1], and the 10T-NWRAM showed 2x performance and 35x leakage improvement with comparable area and active power, when compared with 16nm CMOS SRAM [3][4]. These benefits are attained at a significantly relaxed overlay. Our simulation results showed 100% yield can be achieved in N^{3}ASIC manufacturing for an overlay of ±8nm [5]; this is considerably less stringent than CMOS, which requires an overlay precision of ±3nm at 16nm.

Junctionless cross-nanowire FETs can be used to further simplify manufacturing requirements. In these devices, source, channel and drain regions are uniformly doped without the need for abrupt doping profiles or high thermal budgets. junctionless transistors operate on the principle of channel depletion induced by work-function difference between the metal gate and the doped channel [24]. Given the nanoscale dimensions of the channel cross-section, the channel region can be completely depleted of carriers at zero gate voltage, leading to normally OFF devices. Applying a voltage bias on the metal gate eliminates the work-function difference, turning ON the device.

We have studied junctionless device behavior through detailed 3-D Synopsys Sentaurus process [22] and device [11] simulations. The device structure (Fig. 2A) was created using process simulations considering detailed process effects such as implantation parameters, diffusion temperature, oxide deposition rate etc. Device simulations were carried out to determine carrier transport in the device structure. For device simulations, hydrodynamic charge transport model with

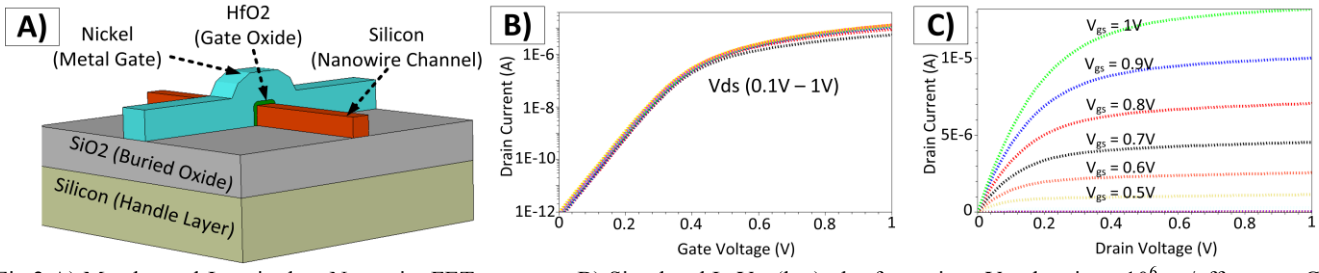


Fig.2 A) Metal-gated Junctionless Nanowire FET structure, B) Simulated I_d-V_{gs} (log) plot for various V_{ds} showing >10^6 on/off current C) Simulated I_d-V_{ds} curve for different V_{gs} showing linear and saturation regimes of operation.

quantum corrections [11] was used to model charge transport accounting for quantum confinement effects. 'OldSlotBoom' bandgap narrowing model [11] was used to calculate band bending, and doping dependent mobility calculation [11] was done to account for highly doped channel. Simulated device dimensions were 16nm (gate length) X 16nm (channel width) X 10nm (channel thickness). HfO_2 gate dielectric with 2nm thickness and Nickel (workfunction = 5eV [16]) gate was assumed. N-type Si nanowire channels were simulated with a sufficiently high doping (2 X 10^{19} dopants/cm^3) to achieve a high on-current.

Results of I_d – V_g simulations (Fig. 2B) validate the expected behavior of cross-nanowire junctionless transistors. At zero gate voltage, drain current is in the order of ~10pA implying a normally OFF condition. As a positive bias is applied, carriers are accumulated into the channel. Above the threshold voltage a conducting path is established and the device is considered ON. Accumulation increases up to the flat-band condition, when the channel concentration reaches the initial doping concentration. ON-current for this device was found to be 14µA, and the threshold voltage was 0.3V. Fig. 2C shows linear and saturation regimes of operation similar to N-type FETs. The high ON-current (14µA), I_{ON}/I_{OFF} ~ 10^6, and adequate threshold voltage (0.3V) implies that the junctionless device meets the noise margin and cascading requirements of N^3ASIC circuits [8]. These results also show that the junctionless transistor with simplified manufacturability is still competitive against conventional NMOS (PTM 16nm NMOS: 15µA I_{ON} [17]).

In addition to not requiring abrupt doping profiles or high temperature anneals, the metal gated junctionless FET also enables a wide range of material choices for gate dielectric and gate electrode to tune device parameters. Additionally, combined with a circuit scheme that does not require two different types of FETs, using junctionless uniformly doped devices enables manufacturing pathways where doping requirements are limited to a single initial wafer-wide doping step, as will be detailed in the next section.

III. N^3ASIC Scalable Manufacturing Pathway

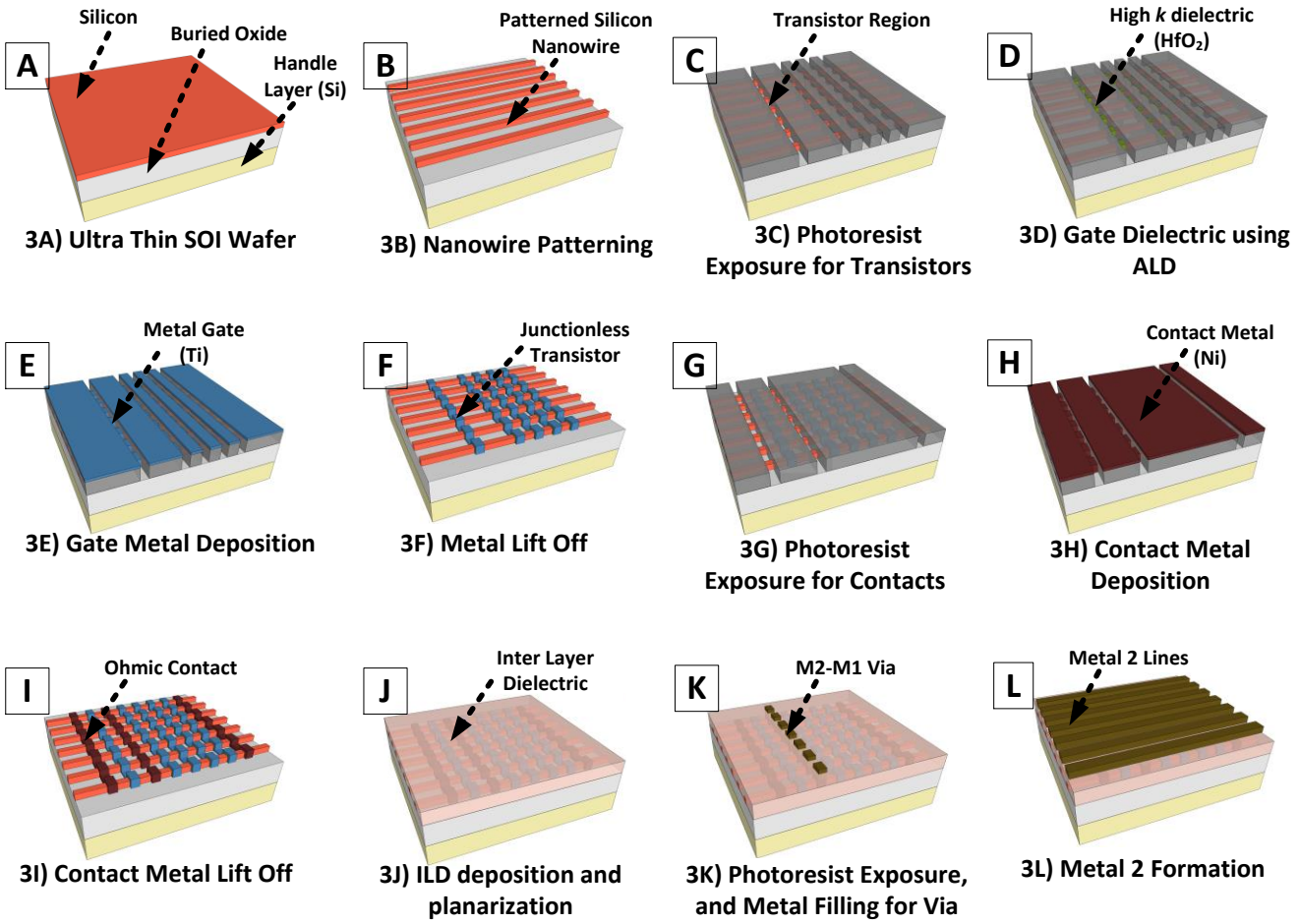
N^3ASICs fabrics with junctionless transistors can be assembled using a bottom-up integration sequence that combines unconventional patterning and photolithography steps while carefully managing overlay requirements. Fig. 3 shows the envisioned manufacturing pathway, where the key steps are initial wafer-wide substrate doping, nanowire patterning, device region masking, dielectric and metal gate deposition, ohmic contact formation for power rails and output vias, interlayer dielectric deposition, and metal stack formation.

A Silicon-on-Insulator (SOI) wafer with an ultra-thin top Silicon device layer is the prerequisite for the N^3ASIC fabric, since junctionless devices require nanoscale channel cross-sections for complete depletion, as discussed in the previous section. For strain application in junctionless devices, a wafer level universal strain can be introduced in silicon. Wafer-level universal strain [12] is sufficient, since N^3ASIC circuits require only one type of junctionless transistors without any doping variation.

In order to dope the silicon layer with dopants (e.g., as for N type, B for P type) initially, a wafer level diffusion doping or ion implantation followed by high temperature annealing can be employed. Fig. 3A illustrates the starting highly doped SOI wafer used in this methodology.

To pattern nanowire arrays on silicon substrate, low cost unconventional patterning steps such as nanoimprint, block copolymer assembly and patterning can be used. Unconventional patterning approaches (e.g., nanoimprint lithography (NIL) [18]) can achieve very high density nanowire-arrays, but suffer from extremely poor overlay alignment. Therefore, in our manufacturing pathway, unconventional patterning approaches are used only in the beginning without any alignment or registration offset [5][13]. All subsequent steps are lithographic and follow lithographic design rules [1].

Nanowire patterning step is followed by transistor region masking and gate material deposition in a gate first process as shown in Fig. 3C, 3D and 3E. An atomic layer deposition technique, where dielectric layer deposition only occurs to silicon surface, is used. A wide range of dielectric materials such as rare-earth oxides Al_2O_3, ZrO_2 etc., can be explored for junctionless transistors, since high temperature material diffusion concerns are not present during junctionless transistor fabrication. Traditional high *k* materials such as HfO_2 can be also used. However, application of HfO_2 would require proper surface preparation by hydrogen-terminated bonds or by taking care of oxygen deficiencies at HfO_2-Si interface to remove defects [14][15]. HfSiON dielectric with high temperature annealing can be also used to maximize device performance [14].



The next steps in the process flow are metal gate work function layer deposition (Fig. 3E) and lift-off (Fig. 3F). Similar to gate dielectric, the material selection choices for junctionless transistors can be many due to low thermal budget. Fig 4 shows range of available metals and metal alloys that can be used for N and P type junctionless transistors. TiN or Ti are two good choices as gate metals for N or P type junctionless devices, respectively.

Metal-silicon Ohmic contact formation steps for power rails and vias are shown in Fig. 3G, 3H and 3I. Titanium-Silicon, Ohmic contacts for N+ doped Silicon and Nickel-Silion Ohmic contacts for P+ doped Silicon are widely used in literature. The same materials can be used for N^3ASICs Ohmic contacts also.

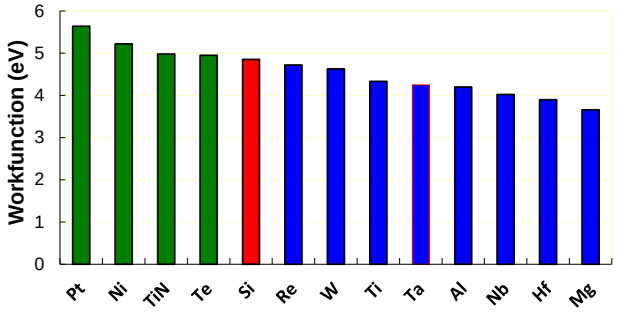


Fig. 4 Ideal metal workfunction (clean surface) [16]

In the next steps, interlayer dielectric will be deposited followed by planarization step (Fig. 3J). A low *k* dielectric material (e.g., Aromatic thermosets, Teflon AF [19]) can be used to make sure interlayer coupling noises are less. For planarization, standard techniques such as chemical mechanical polishing can be used. The next steps in N^3ASIC manufacturing are interconnecting metal stack formations through via filling (Fig. 3K) and metal line definitions (Fig. 3L).

As evident from the above discussions, N^3ASICs manufacturing complexities are significantly less when compared to CMOS; there are no sharp doping profiles, or arbitrary placement of transistors. Moreover, there is no requirement for shallow trench isolation regions, spacers, and EPI contacts as it is in CMOS manufacturing [20].

In the next section we show our experimental prototyping results of N^3ASIC fabric. Prototyping process flow used is similar to that of scalable manufacturing pathway described above.

IV. EXPERIMENTAL PROTOTYPING

We have experimentally demonstrated prototype of N^3ASIC tile structure and validated device assumptions through fabrication and characterization. Electron-beam lithography (EBL) was used to define sub-30nm structures, and to do alignment of metal input gates against nanowire channels.

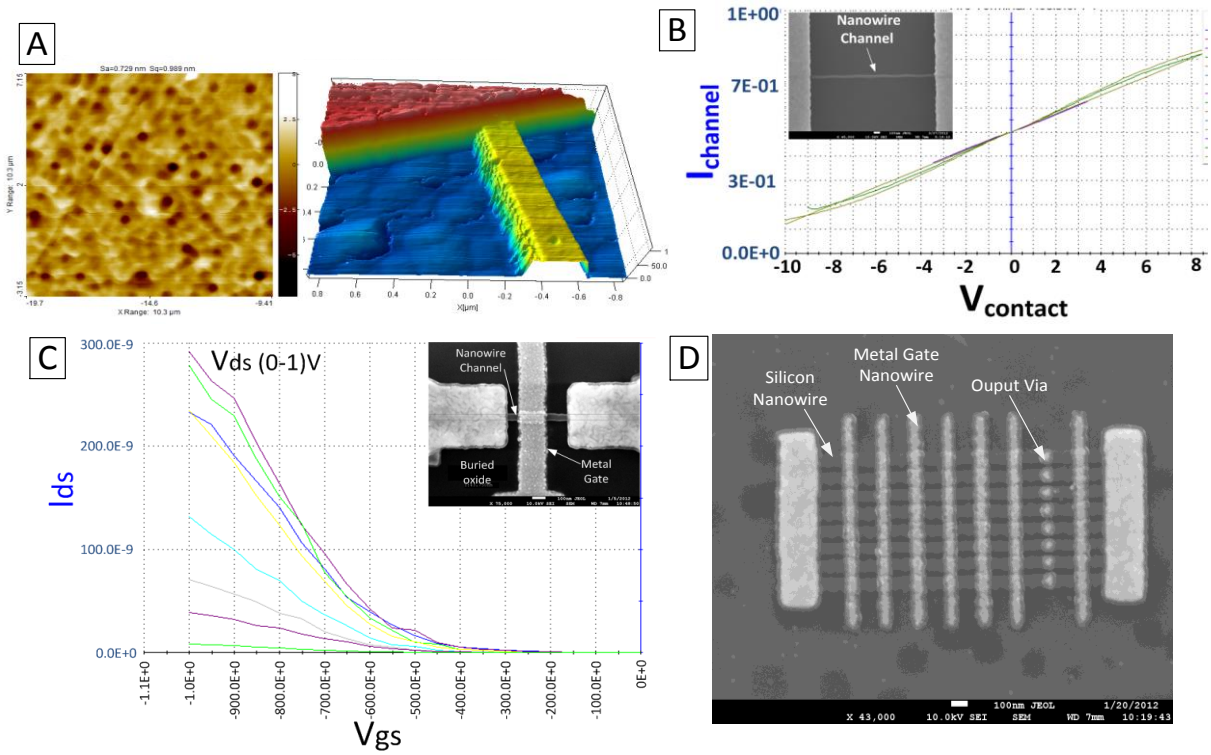


Fig. 5 A) AFM results: less than 1nm surface roughness after RIE thinning (left), 15nm thick Si nanowire on top of SiO_2 substrate (right). B) I-V measurements of nanowire channel showing linear increase in current for wide range of voltages. C) I_d -V_{gs} characteristics of fabricated P-type Junctionless nanowire transistor, the device is normally OFF at 0 V_{gs} , turns ON fully at -1V_{gs} . D) Single logic stage of the fabric, nanowire array with 30nm wide nanowires (horizontal) and 100nm spacing, 30nm wide and 200nm spaced metal gate nanowires (vertical), Vias for output propagation.

The starting wafer was a SOI wafer which had 100nm silicon on top. Wafer level doping was carried out using ion implantation, and thermal annealing. Ion implantation parameters (dopant: Boron, energy: 28KeV, dosage: 10^{14} dopants/cm^2) for P type junctionless transistor was chosen from SRIM [21], process and device simulations [11][22] to achieve required dopant density (10^{19} dopants/cm^3) and to make sure dopants reach bottom 20 nm of the silicon layer. Thermal annealing at 1000° C was carried out for 60 minutes to diffuse dopants and to recrystallize silicon substrate.

The top silicon layer was then thinned to 15nm, as it is a requirement for junctionless transistor operation. A CHF_3, SF_6 recipe was used for this purpose. Nanowire features in this ultra-thinned substrate were then defined using EBL, and a nickel etch mask was used to do nanowire pattern transfer on to buried oxide.

Fig. 5A (left) shows AFM measurements Silicon surface after thinning, the results show that the top Silicon surface is smooth with less than 1nm of surface roughness across a large area. Fig. 5A (right) shows AFM thickness measurement results after nanowire pattern step. A 200nm wide nanowire is shown with 15nm thickness.

Ohmic contacts to P+ doped Silicon nanowires were formed with Nickel-Silicon contacts. The conductivity in these fabricated nanowires and contact resistance was measured using two-probe I-V measurement techniques. Fig. 5B shows excellent Ohmic behavior with linear increase in voltage resulting in linear increase in current. The contact voltage was sweeped from -10V to +8V. The linear I-V behaviors of contact and channel resistance were consistent for nanowires with varying widths: 30nm, 100nm and 200nm.

We fabricated junctionless transistor structures on sub 30nm wide nanowires as shown in Fig. 5C (inset). HfO_2 was used as high *k* dielectric. Prior to HfO_2 deposition, the Si surface was treated with HF solution for cleaning purposes and to terminate Si dangling bonds with Hydrogen. Atomic layer deposition technique was carried out at 150° C using Tetrakis precursor (Tetrakis (dimethylamido) hafnium, $Hf(NMe_2)_4$) to deposit 1.2nm HfO_2. Ellipsiometry measurements were carried out to verify HfO_2 thickness.

Titanium was used as gate electrode, since Titanium's workfunction is sufficient to deplete holes from P-type channel during OFF state (i.e., V_{gs} = 0) of the transistor (Fig. 4). The gate length of these fabricated Ti gated transistors was 200nm.

Three-point probe I-V measurements were carried out to characterize transistor behavior; the measurement result is shown in Fig. 5C. The I_{ds}-V_{gs} characteristics in Fig. 5C accurately depicts junctionless device characteristics, where the workfunction difference between Ti gate and P+ doped Si nanowire channel depletes the channel and the device is normally OFF at 0V V_{gs}. As the negative gate voltages (V_{gs} < 0) are applied, the carriers are accumulated and the channel conducts. These devices have an I_{on}/I_{off} ~ 1000 and threshold

voltage ~ -0.3V. Characterization was done using Keithley 4200 parametric analyzer and Wentworth probe station.

We have fabricated a single stage of N^3ASIC fabric with junctionless transistors at each cross-point as shown in Fig. 5D. The horizontal Silicon nanowires are 30nm in width and 15nm in thickness; each nanowire is spaced by 100nm. The vertical metal gate input nanowires are 30nm in width, and 50nm in thickness; each vertical nanowires are separated by spacing of 200nm. Fig. 5D also shows output Vias that are 200nm in length.

V. Conclusions

N^3ASIC is a new computing fabric that addresses device, interconnect and integration synergistically to simplify critical manufacturing challenges facing CMOS while still achieving efficiency benefits vs. equivalent CMOS designs. Integration of junctionless transistors in N^3ASIC fabric reduces manufacturing complexities further. We detailed TCAD simulation results of junctionless transistor, which showed competitive device metrics with 14μA I_{ON} and $I_{ON}/I_{OFF} > 10^6$. N^3ASICs manufacturing pathway incorporating junctionless transistors was presented and wide range of material choices were discussed. We have shown our recent experimental progress towards a functioning N^3ASIC tile prototype. We successfully validated the junctionless device behavior experimentally. We have shown characterization results of sub-30nm wide P-type junctionless transistor with $V_{TH} \sim -0.3V$ and $I_{ON}/I_{OFF} > 10^3$. We have also shown a fabricated single stage of N^3ASIC fabric with active cross-points.

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