A New Tunnel-FET based RAM Concept for Ultra-Low Power Applications

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Abstract— **Maintaining power scaling trend and cell stability are critical challenges facing CMOS SRAM at sub-20nm technologies. These challenges primarily stem from the fundamental limitations of MOSFETs, and the rigid device doping and sizing requirements of underlying SRAM design. In this paper, we propose a new volatile memory architecture called Tunnel FET based Random Access Memory (TNRAM) that solves CMOS SRAM scaling challenges through integration of ultra-low power Tunnel FETs (TFETs) in a novel circuit style. It is designed to operate with single type uniform transistors to eliminate nanoscale device sizing requirements, and is customized to prevent SRAM like stability concerns. Analytical projections show significant power benefits; 6T-TNRAM has 4.38x lower active power and 174x lower leakage power over HP 6T-SRAM at 16nm technology node.**

Index Terms—**Ultra-Low Power, Tunnel FET, TNRAM, Nanoscale Memory, Noise Margin.**

I. Introduction

The demand for dense, high-performance, low-power and reliable cache memories have led to research on new materials, devices, circuits and integration schemes. However, these directions maintain the underlying 6T-SRAM design with optimizations to boost stability and use new peripheral circuits [1]. In this paper, we introduce a novel concept called 6-Transistor Tunnel FET based RAM (6T-TNRAM) to overcome SRAM's scaling challenges. Only single type uniform N-type TFETs are used in TNRAM design, alleviating SRAM-like requirements for precise doing/sizing; the memory operations are achieved by synchronizing data inputs with non-overlapping clock phases, which mitigate stability concerns. The TNRAM design and operating principle along with ultra-low power operations of TFETs ensure significant power saving compared to SRAM.

II. 6T-TNRAM Architecture

TFETs have ultra-low switching power due to the carrier transport mechanism that primarily relies on band lowering and tunneling (Fig. 1); operating voltage as low as 0.2V has been shown [2]. In addition, the asymmetry of Source and Drain regions can be optimized to have a unidirectional current flow (Drain to Source); this feature is very useful for TNRAM design, since it allows compact realization through sharing of virtual *GND* lines between cells.

The TNRAM architecture and expected behavior are shown in Figs. 2-7. The memory cell is composed of three 2-input dynamic NAND gates (Fig. 2); two of these are used in a cross-coupled manner to store true and complementary values, and a separate NAND gate is used for reading the stored value. Memory operations are synchronized with input clocks: W_0Pre_0, W_0Pre_1, C_0Eva_0 and C_0Eva_1. In order to write '1', the Out_0 is precharged first by turning ON the W_0Pre_0 signal, is followed by $NOut_0$ discharge during W_0Pre_1, C_0Eva_1 clock phases. For writing '1', C_0Eva_0 signal is gated to prevent discharge of Out_0. The evaluate transistors gated by C_0Eva_0 and C_0Eva_1 inputs are shared across multiple cells in a column, and intermediate W_0GND_0 and W_0GND_1 signals act as gated virtual *GND* for each cell (Fig. 3-4).

During idle periods all control signals are switched OFF to minimize leakage, and are periodically turned ON to restore the state. TNRAM behavior is projected through HSPICE simulations in Figs. 5-7; here MOSFETs are used as active devices, and TFET's unidirectional current flow is emulated using voltage controlled resistors.

III. TNRAM Evaluation and Conclusion

Analytical calculations using exact device and interconnect parameters were done at 16nm technology node. Two different TNRAM designs using Ge and $In_{0.53}Ga_{0.47}As$ based TFETs [3][4] were compared with high performance MG-MOSFET [5] based SRAM design. Device parameters were obtained from references [3]-[5], and interconnect parasitics were derived from designed TNRAM (Fig. 3) and SRAM layouts [7]. For all metrics, worst case conditions were considered. Design rules and methodology used are shown in Table 1 and Fig. 7. Results show up to 174x lower leakage power, 4.38x lower active power and 1.6x higher performance (write) with Ge-TFET based TNRAM design at comparable area. The read delay is lower compared to SRAM due to lower drive current of TFETs. These results are indicative of TNRAM's potential for future ultra-low power embedded memories.

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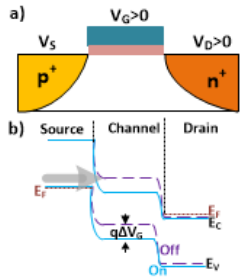

Fig.1. a) TFET schematic, b) band diagrams for On and Off states

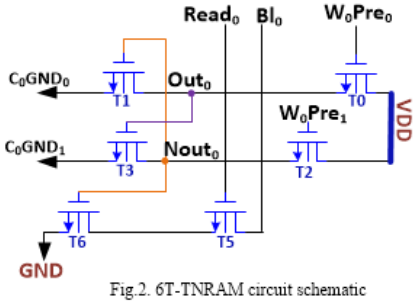

Fig.2. 6T-TNRAM circuit schematic

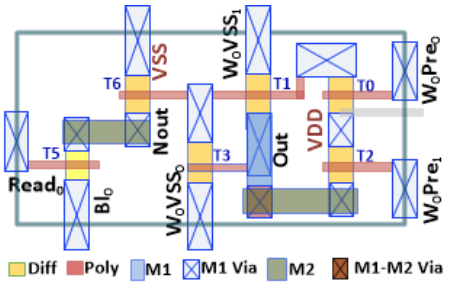

Fig.3. 6T-TNRAM cell layout

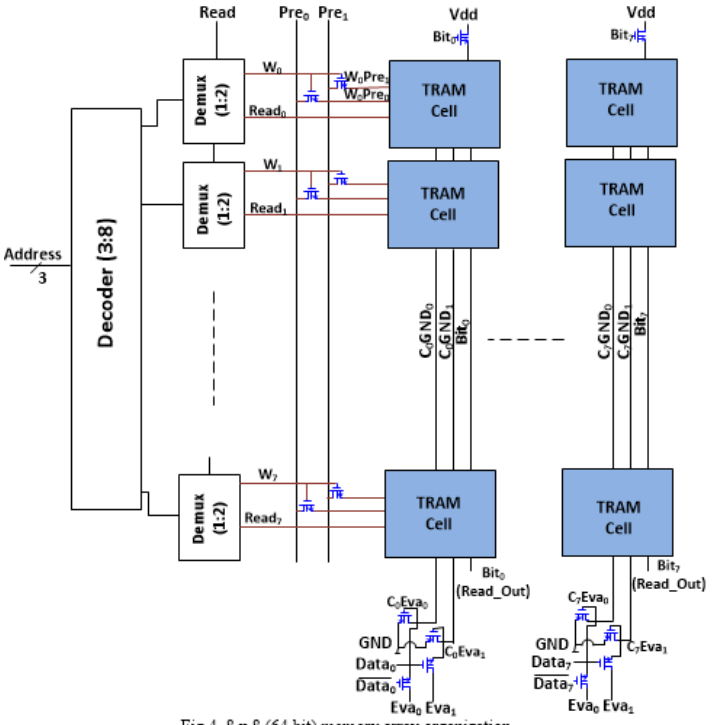

Fig.4. 8 x 8 (64 bit) memory array organization

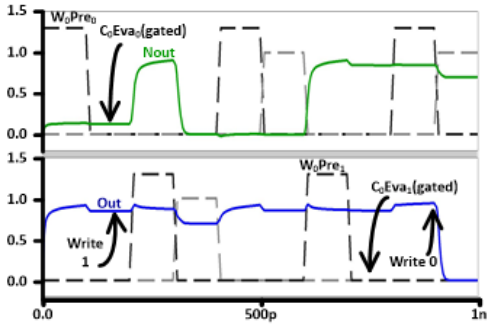

Fig.5. Simulated waveforms (Write operation)

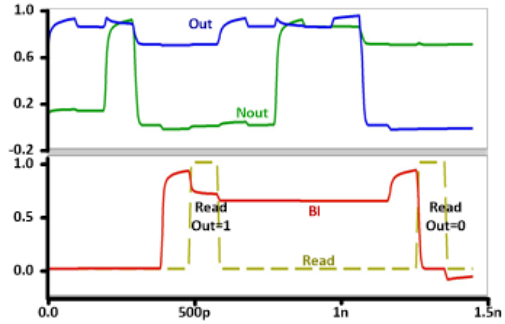

Fig.6. Simulated waveforms (Read operation)

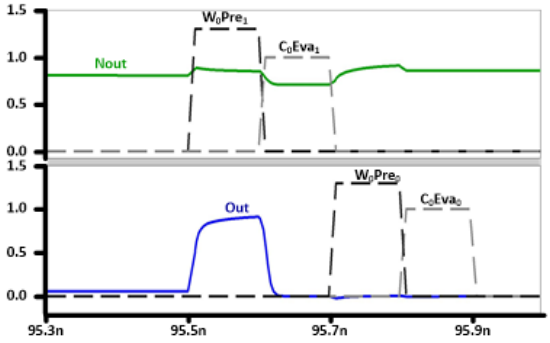

Fig.7. Simulated waveforms (Restore operation)

6T-TRAM

Write delay: $2.3 * [(R^{T3}+R^{TC0EVA1}) * (C_G^{T6}+C_G^{T1}+C_P^{T3}+C_P^{T2}) + R^{TC0EVA1} * (C_P^{T3}+C_P^{TC0EVA1})]$

Read delay: $2.3 * [(R^{T5}+R^{T6}) * (C_P^{TBit}+8*C_P^{T5}+C^{Bl}) + (C_P^{T5}+C_P^{T6})*R^{T6}]$

Active power: $(C_P^{TBit}+8*C_P^{T2}+C^{Bl})*VDD^2*\alpha*f$

Leakage Power: $0.125*[VDD^2 / (R_{off}^{TBit}+0.125*R_{off}^{T5})] + VDD^2 / (R_{off}^{T2}+R_{off}^{T3}+R_{off}^{EVA1}) + VDD^2 / (R_{off}^{T0}+R_{off}^{EVA0})$

6T-CMOS

Write delay: $2.3 * [0.5*(C_G^{PU0}+C_G^{PD0}+C_P^{PU1}+C_P^{PD1}+C_P^{PS1})*R^{PS1} + R^{PU0}*(C_G^{PU1}+C_G^{PD1}+C_P^{PU0}+C_P^{PD0}+C_P^{PS0})]$

Read delay: $2.3 * [(8C_P^{PS1}+C^{Bl})*(R^{PS1}+R^{PD1})]$

Active power: $(8C_P^{PS1}+C^{Bl})* VDD^2*\alpha*f$

Leakage power: $VDD^2/R^{PU0}+VDD^2/R^{PD1}+VDD^2/R^{PS0}$

Notations:

R^{Tx}: Tx resistance, C_G^{Tx}: Tx gate capacitance, C_P^{Tx}: Tx parasitic capacitance, C^{Bl}: bitline capacitance/cell, **PUx:** pull-up transistor (x: 0 or 1, represents left or right symmetric transistor), **PD:** pull-down transistor, **PS:** pass transistor, α: activity factor, f=1/(read delay)

Fig. 8. Evaluation Methodology

Table 1. Design rules at 16nm

	Length (nm)
N+/P+ spacing	37.54
M1 half pitch	28.88
M2 half pitch	28.88
Via spacing (nm)	28.28
M1-Poly spacing	5
TFET L/W	20/20
MOSFET L/W (2D-Nominal)	20/26

Design rules are similar to lower bound shown in [1]

Table 2. Comparisons between HP 6T-SRAM, 6T-TNRAM with Ge based TFETs, and 6T-TRAM with $In_{0.53}Ga_{0.47}As$ based TFETs

	SRAM	TRAM (Ge)	TRAM ($In_{0.53}Ga_{0.47}As$)
Area (μm^2)	0.042	0.071	0.071
Write Time (ps)	20.3	12.6	14.2
Read Time (ps)	12.5	59.5	142.5
Active Power (nW)	86	19.6	6.6
Leakage Power (nW)	5.23	0.03	0.94

VDD=0.5V; Lg = 20nm; Nominal W= 20nm for TFETs, and 78nm for MG MOSFETs; TFET-Ge and TFET-$In_{0.53}Ga_{0.47}As$ parameters from [3] and [4]. PTM-MG HP transistors [5] for SRAM; 2x, 1.5x and 1x sizing for PD, PS and PU transistors. α = 0.02; C_o = ½ C_G for TFETs and C_o = 1/6 C_G for MG-MOSFETs. Bl length for 8 cells in a column was considered.