Impact of Process Variation in Fault-Resilient Streaming Nanoprocessors

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Abstract. We show results from ongoing work studying the interaction of process variation and built-in fault resilience intended to handle defects. We find that built-in fault resilience decreases the negative effects of process variation on a streaming nanoprocessor design.

Keywords: nanoscale processor, process variation, defect tolerance.

1 Background

All nanoscale circuit architectures include a defect-tolerance mechanism to handle the high defect rates expected with bottom-up manufacturing techniques. This is required to achieve acceptable yield, as has been extensively studied. One such mechanism is built-in fault resilience, where logic is added to allow the circuit to function even if some of its components are not functioning correctly. Some proposed systems use reconfiguration to work around defects, but built-in fault resilience may be required to tolerate faults from other sources.

Another major issue with nanoscale circuits, as with CMOS circuits today, is process variation. Process variation leads to large variation in delay, which may cause incorrect function of the system due to missed deadlines and also makes it difficult to achieve high performance.

We are using WISP-0, a simple 5-stage streaming processor design, based on the NASIC nanoscale fabric architecture, to explore the impact of process variation on circuits with built-in fault resilience. NASIC is a tiled 2-D grid-based circuit fabric using a dynamic circuit style. For more information on NASIC and WISP-0, please see [1].

2 Simulation Results

We have used results from the literature [2] [3] [4] [5] to implement a timing model for NASIC. We use the WISP-0 design in our simulations so as to gauge the effects on a processor. In order to capture the typical behavior, we use the Monte Carlo method, picking the parameter values used for each wire and transistor from a distribution. We use a Gaussian distribution with a variation of

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$3\sigma = 60\%$ for each parameter, which is higher than reported by nanoscale device and materials researchers. Some of the parameters varied are the diameter of the nanowires, the resistivity of the wires, the contact resistance with the microscale wires, the pitch of the grid, and the thickness of the gate oxide.

For each set of parameter values, the minimum delay at which the processor can achieve correct results is determined through simulation. Circuits which cannot operate correctly at any speed are not considered in the delay statistics.

The type of fault resilience used is integrated error correction (IEC) based on Hamming codes combined with 2-way redundancy (IEC). Defects considered are both stuck-on and stuck-off transistors, with the proportions assumed to be 90% stuck-on due to the structure and devices used in NASIC. For more details about the fault model and fault resilience technique, see [1].

Table 1. Delay per cycle with and without process variation (in picoseconds)

No Variation	With Variation ($3\sigma = 60\%$)		
No defects	No defects	5% defects	10% defects
182.15	178.47	182.4	184.41

In a traditional circuit, we would expect to see the typical case be slower than what could be achieved without process variation. However, as can be seen in Table 1, the mean delay for WISP-0 with fault resilience is instead decreased. This decrease in delay is due to the IEC handling timing faults, thus allowing the speed to be pushed further. Since only a limited number of faults can be tolerated by each stage, as the defect rate goes up, the delay increases as well.

Circuits with built-in fault resilience clearly also have some tolerance for process variation. We are working on techniques to further decrease the impact of process variation on performance, especially in the presence of defects, and to increase the overall performance of NASIC circuits.

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