

# Power-Delivery Network in 3D ICs: Monolithic 3D vs. Skybridge 3D CMOS

Jiajun Shi, Mingyu Li and Csaba Andras Moritz

Department of Electrical and Computer Engineering

University of Massachusetts, Amherst, MA, USA

[jiajun@umass.edu](mailto:jiajun@umass.edu), [andras@ecs.umass.edu](mailto:andras@ecs.umass.edu)

**Abstract**—Design for power-delivery network (PDN) is one of the major challenges in 3D IC technology. In the typical layer-by-layer stacked monolithic 3D (M3D) approaches, PDN has limited accessibility to the device layer away from power/ground source due to limited routability and routing resources in the vertical direction. This results in an incomplete and low-density PDN design and also severe IR-drop issue. Some improved M3D approaches try to enlarge design area to create additional vertical routing resources for robust and high-density PDN design. However, this leads to degradation of design density and in turn diminishes 3D design benefits. Skybridge 3D CMOS (S3DC) is a recently proposed fine-grained 3D IC fabric relying on vertical nanowires that presents a paradigm shift for scaling, while addressing critical challenges in 3D IC technology. Skybridge’s core fabric components provide a greater degree of routing capability in both horizontal and vertical directions compared to other 3D approaches which can fully maintain the 3D design density while enabling a robust PDN design. In this paper, we present the PDN design and evaluate the IR drop in S3DC vs. the state-of-the-art transistor-level monolithic 3D IC (TR-L M3D). The typical TR-L M3D approach that can only use low-density PDN shows a severe IR-drop which is out of the standard IR-drop budget. The improved TR-L M3D version that can use high-density PDN meets the requirement of standard IR-drop budget ( $<5\%*VDD$ ) but loses up-to 25% power efficiency and 20% density benefits over 2D compared to the typical TR-L M3D. On the other hand, S3DC maintains its significant benefits over 2D (2.7x power efficiency and 9x density) while using a robust PDN design that has negligible IR-drop ( $<2\%*VDD$ ).

**Index Terms**— Routability, 3D ICs, IR-Drop, Power delivery network, 3D power and performance characterization

## I. INTRODUCTION

Three-dimensional integrated circuits (3D ICs) are emerging as a promising technology to advance scaling due to fundamental challenges in 2D that stem from device scaling limitations. Conventional fine-grained 3D ICs with layer-by-layer stacking using Monolithic Inter-layer Vias (MIVs) [1] have been explored in recent years for continuing technology scaling. However, this Monolithic 3D (M3D) technology still relies on conventional 2D CMOS device, circuit and interconnect mindset showing only incremental benefits while adding new challenges such as thermal management [2], manufacturing [3] and routability issues [4].

The design for power-delivery network (PDN) is one of the major challenges in M3D which is caused by the routability issue. Due to limited routing capacity in vertical direction, PDN on top metal layers has poor accessibility to the device layer away from the power source. This leads to severe IR-drop in this device layer. In gate-level (G-L) M3D IC [5], large number of MIVs need to be used in cell-to-cell communication between top- and bot-tier while limited

number of MIVs are used in the PDN’s vertical routing to the bot-tier. Therefore, taking some cell-to-cell routing resources for PDN routing or enlarging design area to add routing resource for PDN, is the only way to achieve a robust and high-density PDN design in G-L M3D [5]. In the typical version of transistor-level (TR-L) M3D [6], top-tier’s high-density routing creates blockages, which limit PDN’s vertical routing access to bot-tier and results in an incomplete and low-density PDN design. In the improved TR-L M3D version [7], larger cell footprint is used to add additional vertical routing resource for PDN’s access to bot-tier. Overall, in both G-L and TR-L M3D approaches, the insertion of a robust PDN design would impact 3D cell-to-cell routing density which in turn diminishes the benefits over 2D design.

Skybridge 3D CMOS (S3DC) [8] is a fine-grained 3D IC fabric that uses vertically-stacked gates and 3D interconnections composed on vertical nanowires to yield orders of magnitude benefits over 2D ICs. This 3D fabric fully uses the vertical dimension instead of relying on a multi-layered 2D mindset. Its core fabric aspects including device, circuit-style, interconnect and heat-extraction components are co-architected considering the major challenges in 3D IC technology. In S3DC, the 3D interconnections provide greater routing capacity in both vertical and horizontal directions compared to conventional 2D and 3D ICs [9], which enables its ultra-high density design and significant benefits over 2D. Also, the improved routing capacity in S3DC is beneficial for a robust and high-density PDN design whose presence would not impact or create blockages on the 3D cell-to-cell routing.

In this paper, we present the PND design in S3DC that fully uses the routing capacity in S3DC. We use two large-scale benchmark circuits for IR-drop evaluation: the Advanced Encryption Standard (AES) core and the Low Density Priority Check (LDPC) core. A bottom-up IR-drop analysis was performed by combining Sentaurus TCAD [10] based evaluation of fundamental fabric components and Cadence Voltus [11] based circuit-level PDN evaluation. The S3DC’s PDN design is compared to both low-density and high-density PDN designs in the state-of-the-art M3D approach (TR-L M3D) using uniform 16nm technology node. The results show the typical TR-L M3D that only has low-density PDN has severe IR-drop in bot-tier which is out of standard IR-drop budget while the improved TR-L M3D with high-density PDN and our S3DC can meet the requirement of standard IR-drop budget ( $<5\% VDD$ ). However, the TR-L M3D with high-density PDN has reduced benefits over 2D (25% power efficiency and 18% density in LDPC circuit, 16% power efficiency and 20% density in AES circuit) compared to the typical TR-L M3D approach, while adding high-density PDN in S3DC has no impact on S3DC’s power efficiency and density benefits over 2D.

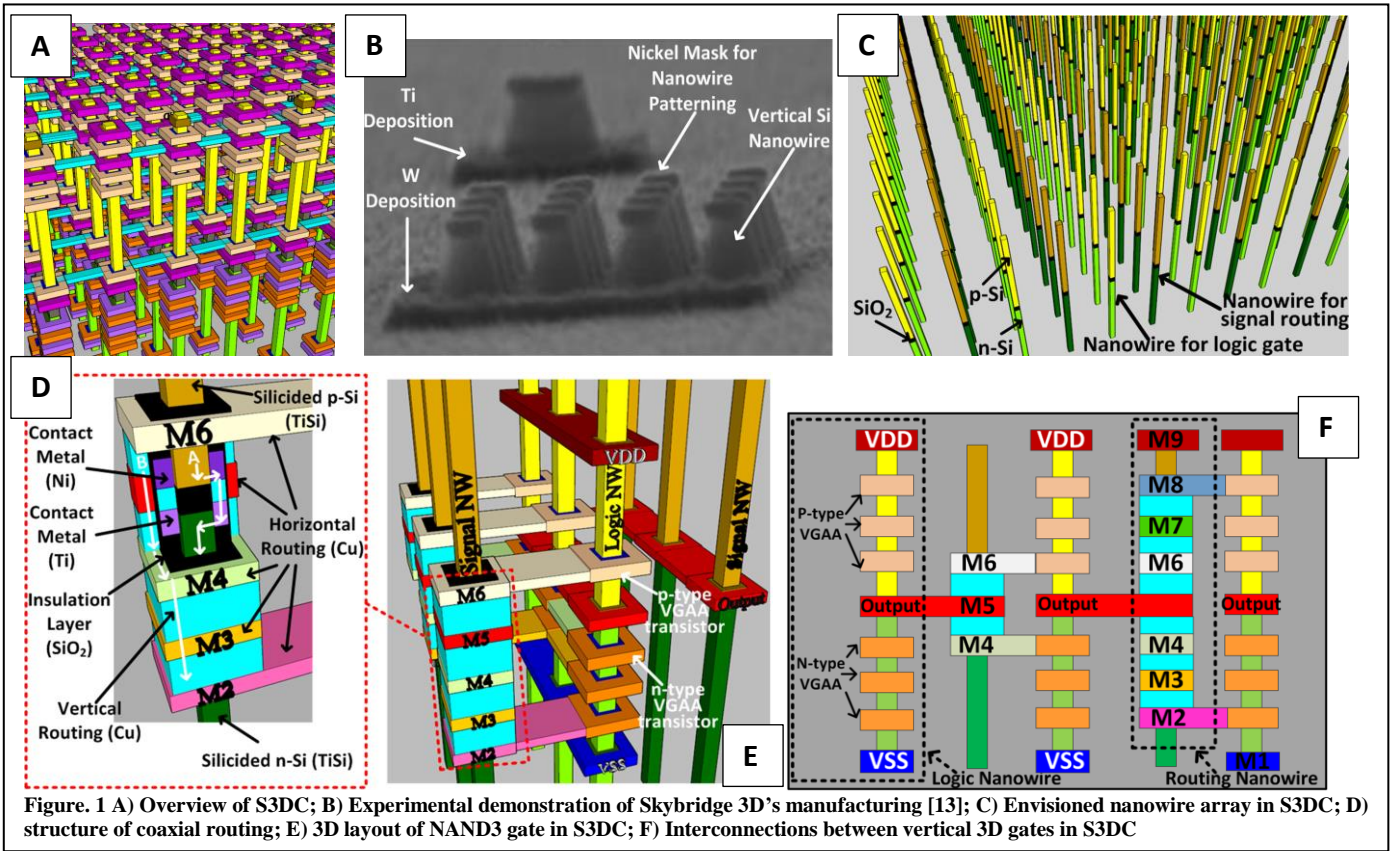


Figure. 1 A) Overview of S3DC; B) Experimental demonstration of Skybridge 3D's manufacturing [13]; C) Envisioned nanowire array in S3DC; D) structure of coaxial routing; E) 3D layout of NAND3 gate in S3DC; F) Interconnections between vertical 3D gates in S3DC

## II. OVERVIEW OF SKYBRIDGE

Skybridge-3D-CMOS (S3DC) is a fine-grained 3D integration [17], designed with a 3D fabric-centric mindset and providing an integrated solution for all core technology challenges. It expands the fundamental concepts original to Skybridge [7] while realizing a vertically-integrated CMOS circuit style for the first time. Fig. 1A shows the envisioned S3DC; it is built with a regular array of uniform vertical dual-doped nanowires (See Fig. 1C); all active components and structures are vertically composed by selective material deposition around nanowires. Detailed manufacturing pathway for S3DC and experimental demonstrations are discussed in [10]. Fig. 1B shows the experimental demonstration of the key manufacturing steps for deposition.

Each dual-doped nanowire has p-type doped silicon on the top-half, n-type doped silicon on the bot-half and a dielectric layer in-between for insulation (See Fig. 1C). An inter-layer contact structure is designed to allow signal routing between n- and p-regions bypassing the dielectric layer between them (See Fig. 1D). Details of the contact structure and resistance evaluation are presented in [13]. The nanowire array consists of rows of logic nanowires and rows of routing nanowires (See Fig. 1C). The logic nanowire is used in logic gate implementation. Core components including n-type and p-type Vertical Gate-All-Around (n-VGAA and p-VGAA) junctionless transistors [18], are stacked on n-type doped and p-type doped regions of each logic nanowire to implement complementary logics of static-logic gates. The device structure and selected materials of n- and p-VGAA junctionless transistors are detailed in [18]. The routing nanowire is used as vertical routing component and has silicided n- and p-type silicon regions (TiSi) for low-resistivity wiring. There are additional routing components

used to enable 3D interconnection and good routability such as bridges and coaxial routing structures. Bridges are metal lines used as horizontal routing metal to form links between adjacent vertical nanowires (See Fig. 1E-F), and span the required distance by hopping over intermediate nanowires. The S3DC fabric is designed with various horizontal metal layers that are vertically stacked along nanowires with uniform thickness and vertical spacing (See Fig. 1F). The coaxial routing structure consists of concentric metal shell around a routing nanowire separated by dielectric (See Fig. 1D). Signals can go through the metal shell layer or the routing nanowire. Fig.1D shows an example: signal A is carried by the routing nanowire and signal B is carried by the metal shell; the coaxial routing structure allows signal B to hop the nanowire and continue its propagation through horizontal metal layer (Bridge). Coaxial routing is enabled by specially-configured material structures for both insulating oxides and contact metal.

Fig. 1E shows the layout of a 3-input 3D NAND gate that is built with 9 nanowires. 3 logic nanowires with 6 stacked VGAA transistors are used for logic implementation. 6 routing nanowires with coaxial routing structures are used for creating input/output pins of the NAND3 gate. In total, 9 horizontal metal layers (M1-M9) are used in the design of S3DC standard cell (See Fig. 1F): M9 is used to place VDD rails which consist of bridges and bridge-to-nanowire contacts, VSS rails with similar structure are placed in M1, output port is created by M5 with an inner connection to the inter-layer contact structure of logic nanowire, n-VGAA transistors are placed in three layers M2-M5 and p-VGAA transistors are placed in three layers M6-M8. The feature sizes of contact metal, bridge, VGAA transistors and the nanowire pitch are designed following the design rules as described in [17]. Additional metal layers (M10-M11) are

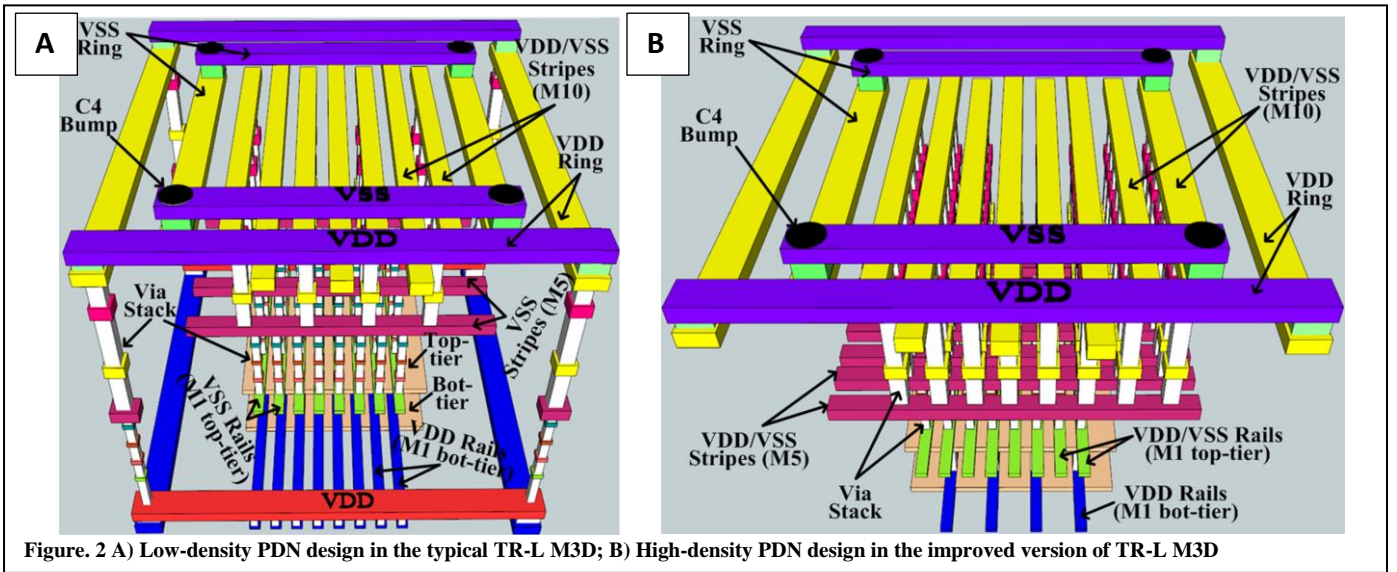


Figure. 2 A) Low-density PDN design in the typical TR-L M3D; B) High-density PDN design in the improved version of TR-L M3D

added on the top of nanowires array to provide necessary routing resources in PDN and clock tree design.

### III. DESIGN OF POWER DELIVERY NETWORK

#### A. PDN Design in TR-L M3D

The PDN design in TR-L M3D follows the standard PDN design techniques which use topmost metal layers for global wires, one intermediate metal layer and VDD/VSS rails in M1 (See Fig. 2A). First, the power and ground signals are fed from the C4 bumps to the VDD and VSS stripes in topmost metal layers (M10-11). These power stripes also have ring connections at the periphery (See Fig. 2A) for lower resistance. Then, the VDD/VSS signals are delivered to the stripes in the intermediate metal layer (M5) by via stacks. These stripes have a finer pitch than the top metal layers (Fig.

2A). The stripes in the intermediate metal layer deliver VDD/VSS signals to local VDD/VSS rails that feed power to standard cells (Fig. 2A). In TR-L M3D, the local VSS and VDD rails are separated and placed into two tiers.

In the typical TR-L M3D approach [6], each standard cell is partitioned into two tiers; the pull-up network (PMOS) with its VDD rail is placed in bot-tier and the pull-down network (NMOS) with its VSS rail is placed in top-tier. The pull-up network exactly aligns with the pull-down network for optimal cell footprint shrinking. However, the VDD rails in bot-tier are thus blocked by the VSS rails in top-tier which leads to poor via accessibility to the VDD rails from intermediate metal layer in top-tier. Therefore, the typical TR-L M3D can only implement a low-density PDN design (Fig. 2A) where VSS rails of cells are connected to its ground source by a network of high-density stripes and via stacks and VDD rails of cells are only connected to its power source by a limited number of via stacks that directly connect the VDD rails to the rings at the periphery of the design block (See Fig. 2A). It is an intrinsic drawback in TR-L M3D that the top-tier's routing creates blockage on the vertical routing access to bot-tier, which in turn limits the communication between top- and bot-tier [6]. In [7], the improved version of TR-L M3D uses larger cell footprint to provide additional vertical routing resource for access to the bot-tier. In this approach, each 3D standard cell has both VSS and VDD rails in M1 of top-tier which can connect to VDD/VSS sources by standard PDN structure (See Fig. 2B). The VDD rails in bot-tier are aligned with the VDD rails in top-tier and connected by via stacks. It enables a high-density and robust PDN design where both VDD and VSS rails of cells are connected to their power/ground sources by a network of high-density stripes and via stacks. However, the major drawback is the footprint of 3D cell is increased due to the use of additional area for inserting VDD rails which impacts the design density and in turn diminishes the 3D benefits.

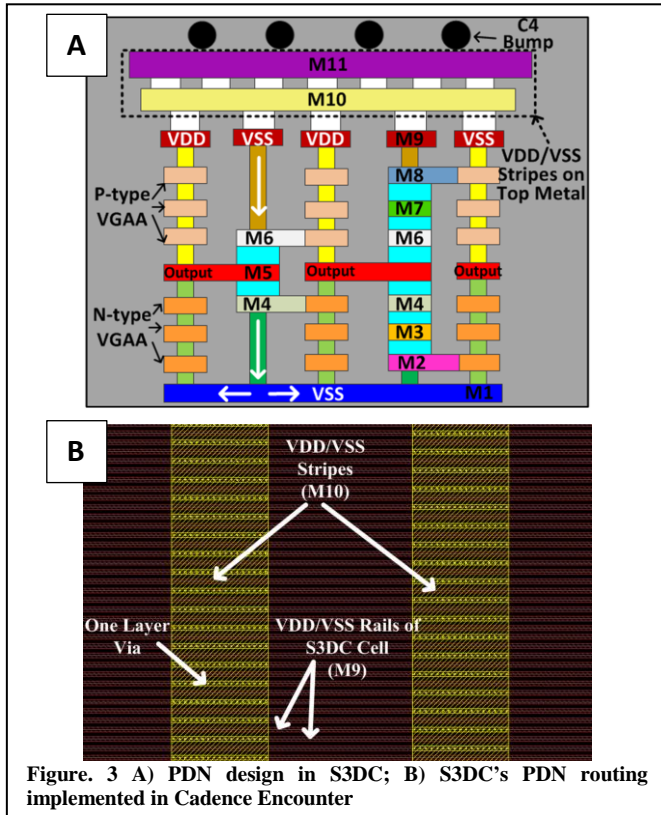


Figure. 3 A) PDN design in S3DC; B) S3DC's PDN routing implemented in Cadence Encounter

#### B. PDN Design in S3DC

S3DC fabric uses vertical nanowire based 3D gates for high-density 3D implementation instead of stacking multiple layers of 2D dies. As shown in Section II, stacking VGAA transistors and contacts on vertical nanowires enables a vertical cell design that has VDD rails on top metal layer M9

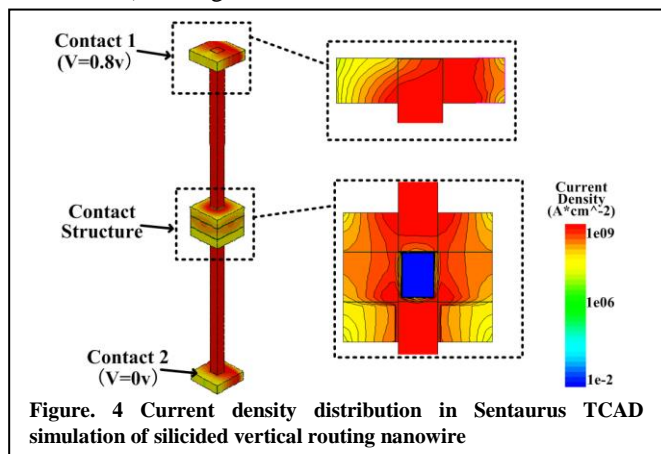
and VSS rail in M1. Therefore, the VDD rails in M9 can be easily connected to VDD stripes in top most metal layers (M10-M11) without using any intermediate metal layer. Also, the coaxial routing structure can provide significantly improved routability in vertical direction which enables high-density via connections between VSS rails in M1 and VSS stripes in the topmost metal layer. Fig. 3.A-B show the detailed PDN design in S3DC: the VDD/VSS stripes with rings are placed in M10-M11 which are added on top of the nanowire array and connected with C4 bumps; VDD rail (M9) of each standard cell is connected to VDD stripes (M10) using only one via layer; VSS signals are delivered from VSS stripes in M10 to each VSS rail that are on the top (M9) of each routing nanowire row; the routing nanowires deliver the VSS signals to the VSS rails of standard cells in M1. In this PDN design, the routing resources of M9/M1 and the vertical routing nanowires (inner routing layer of coaxial routing structure) are fully used for PND routing. The horizontal routing resources of M2-M8 and the vertical routing resources provided by the outer metal shell layer of coaxial routing structure are used in cell-to-cell 3D routing. This way, the cell-to-cell routing and PDN routing are completely separated and have no routing impact or blockage to each other. Considerable vertical routing resources can thus be used to design a robust and high-density PDN.

#### IV. IR-DROP EVALUATION

##### A. Design and Analysis Methodology

Detailed IR-drop analysis was performed in large-scale benchmark circuits. The gate-dominated design AES and interconnect-dominated design LDPC were chosen for benchmarking. The benchmark circuits are implemented in both TR-L M3D and S3DC with uniform 16nm technology node. For both TR-L M3D and S3DC, the design and analysis use commercial CAD tools and encompass all steps from device characterization, RTL synthesis, PDN design, cell placement and routing, to system-level IR-drop evaluation.

The design of S3DC uses the device-to-circuit CAD flow published in [9]. First, we prepared basic design kit of S3DC that includes detailed effects of material choices, confined dimensions, nanoscale device physics, and associated 3D interconnect design rules and RC extraction table. Then the standard ASIC design flow was performed to generate the PDN designs for the benchmark circuits. In this step, the PDN design just includes the VDD/VSS paths from stripes in M10/M11 to the rails in M9. The VSS delivery paths (from M9 to M1) through silicided vertical nanowires were not



implemented in this step since the design tool is not able to implement the coaxial routing structure that contains two layers of vertical routing. In the CAD design stage, only the outer metal shell layer of the coaxial structure was implemented by the vertical via stack between M1 and M9 and used in the cell-to-cell routing. The inner layer of coaxial routing structure (silicided vertical nanowire) which is used for the VSS delivery path from M9 to M1 is not included in the design stage but will be later added into the parasitic extraction results after the design stage in order to capture the full design that contains both inner and outer routing layers. We then performed Sentaurus TCAD [10] to capture the series resistance of the silicided p-type nanowire, inter-layer contact structure and silicided n-type nanowire in a vertical routing nanowire (See Fig. 4). We directly added this resistance value into the extraction results of each VSS delivery paths after the parasitic extraction stage of the full design, since in S3DC adding the PDN routing would not change designed cell-to-cell routings. This way, the updated extraction results can fully capture the parasitics of the S3DC design that has cell-to-cell routing and PDN routing in parallel in the coaxial routing structure. At last, we performed static IR-drop analysis based on the extracted results using Cadence Voltus [11].

The methodology in [6] was used in the design of TR-L M3D. First, design kit was prepared based on a modified Nangate15nm PDK [18]. As discussed in Section III.A, the TR-L M3D with low-density PDN uses different 3D cell structure compared to TR-L M3D with high-density M3D. We created 3D cell library versions for both TR-L M3D approaches. Next, the ASIC flow shown in [6] was used to encompass all steps of benchmarking from RTL to GDS layout. The design was then extracted for IR-drop analysis in Cadence Voltus [11]. Also, we performed IR-drop analysis for PDN design in 2D CMOS using Nangate 15nm PDK [18]. The PDN designs in TR-L M3D and 2D CMOS use the same density of VSS/VDD power stripes in intermediate layer (M5) and topmost metal layers (M10-M11) for fair comparison. The pitch and placement of C4 bumps follow the standard design rules shown in [5].

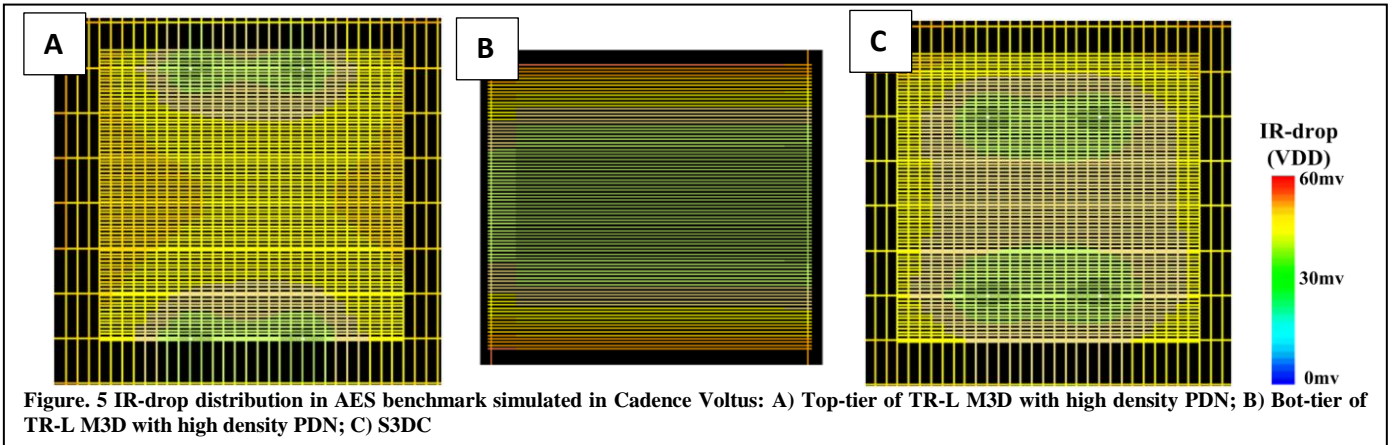
##### B. Results and Comparison

Fig. 5.A-C shows the VDD IR-drop distribution of AES benchmark in TR-L M3D and S3DC. S3DC even has better IR-drop compared to the TR-L M3D with high-density PDN which is attributed to S3DC's significant routing resource that used in the PDN design.

Table I shows the average IR-drop in both LDPC and AES benchmarks. For VSS signal, both TR-L M3D and S3DC are within standard IR-drop budget ( $<5\% \cdot VDD$ ). For VDD signal, the TR-L M3D with low-density PDN is out of standard IR-drop budget. TR-L M3D with high-density PDN has no IR-drop issue in VDD signal; it shows a 3x lower

Table I Average IR-drop (Unit: mv)

Technology	LDPC (VDD=0.8v)		AES (VDD=0.8v)	
	VDD	VSS	VDD	VSS
2D CMOS	22	27	32	38
TR-L M3D (low-density PDN)	62	21	78	32
TR-L M3D (high-density PDN)	21	23	31	34
S3DC	7	14	12	18



VDD IR-drop in LDPC and a 2.5x lower VDD IR-drop in AES compared to the TR-L M3D with low-density PDN. S3DC even shows 3x lower VDD drop in LDPC and 2.6x lower VDD drop in AES compared to TR-L M3D with high-density PDN. Overall, both TR-L M3D with high-density PDN and S3DC can meet the requirement of standard IR-drop budget. Also, it can be observed that AES benchmark always has larger IR-drop compared to the LDPC benchmark. This is caused by the huge number of cells in AES core which leads to large total current flowing through PDN. However, an S3DC cell has significantly reduced cell parasitics [8], which results in cell power efficiency followed by total current reduction. This is a secondary factor that contributes to S3DC's lower IR-drop in comparison to TR-L M3D as well as 2D.

## V. IMPACT ON HIGH-DENSITY 3D ROUTING

### A. Routing Blockage and Congestion

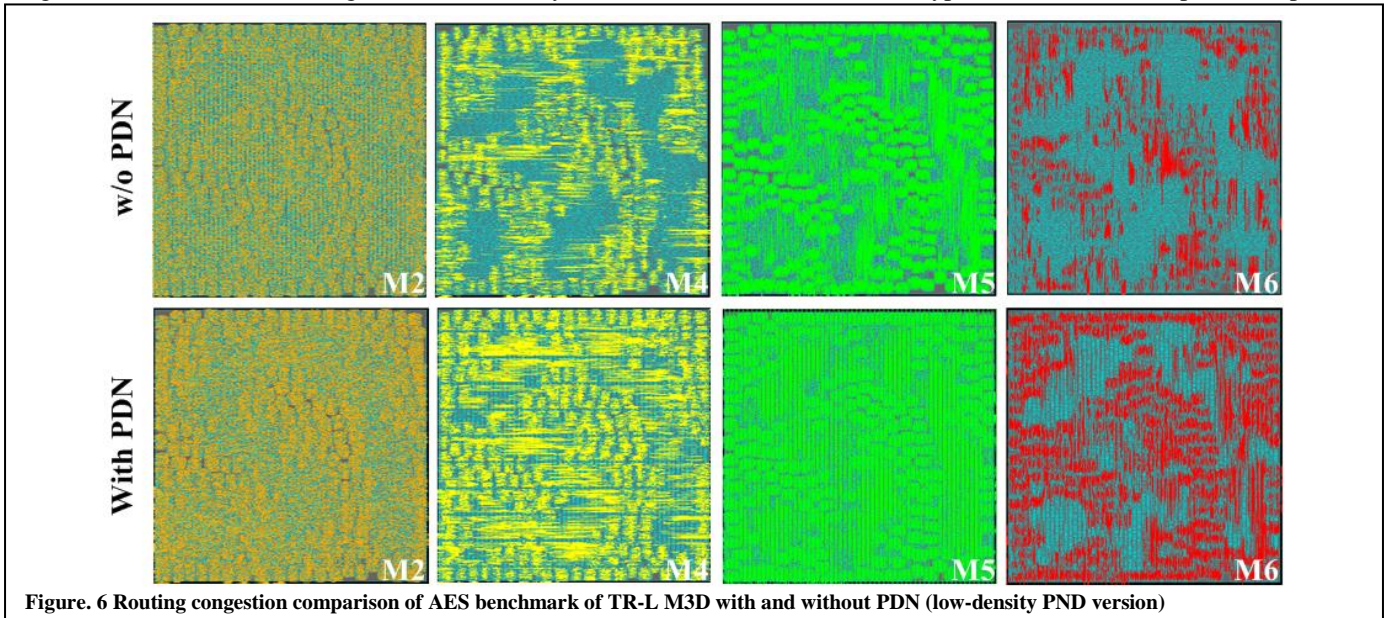
In conventional 2D CMOS technology, the presence of PDN creates certain routing blockages on cell-to-cell routing (cell-to-cell routing is designed after PDN design). Therefore, in conventional 2D design, the trade-off between PDN robustness and cell-to-cell routing efficiency needs to be carefully addressed. In M3D ICs, the cell-to-cell routing has higher (2x) routing density than 2D CMOS, which means the insertion of PDN results in more blockages and heavier congestion on cell-to-cell routing. This would easily lead to a

non-optimal design which has severely increased total wire length and caused degradation of 3D design benefits. Fig. 6 shows the routing of M2, M4, M5 and M6 in the AES benchmark of TR-L M3D with and without PDN (low density PDN). It can be observed that the presence of VDD/VSS stripes in M5 leads to extreme busy routing in M5. The cell-to-cell routing in M6 also becomes much denser due to the heavy routing congestion in M5. Additionally, the presence of via stacks (V1-V5) of PDN creates severe blockage and results in denser routing in M2 and M4 compared to the design without PDN. In the TR-L M3D with high-density PDN, the PDN routing would have more impact on cell-to-cell routing.

In S3DC, the coaxial routing structure can provide 2 layers of vertical routings (See Fig. 1D); the PDN uses the inner layer (silicided nanowire) and the cell-to-cell routing uses the outer layer (the metal shell around a nanowire). This way, the PDN routings are completely separated from cell-to-cell routing and have no routing blockage on cell-to-cell routing. Thus, in S3DC the PDN insertion has no impact on 3D cell-to-cell routing. Also, sufficient routing resource can thus be provided for a robust and high-density PDN design that meets the requirement of the standard IR-drop budget.

### B. Requirement of Routing Resource

Compared to the blockage issue, the severe IR-drop in bot-tire is a more important issue in M3D. As discussed in Section III, in the typical TR-L M3D the power stripes have



**Table II** Benchmarking Results

Technology	LDPC (66K cells)					AES (188K cells)				
	Foot-Print (mm <sup>2</sup> )	Best Frequency (GHz)	Wire Power (mW)	Cell Power (mW)	Total Power (mW)	Foot-Print (mm <sup>2</sup> )	Best Frequency (GHz)	Wire Power (mW)	Cell Power (mW)	Total Power (mW)
2D CMOS	0.084	2	133.3	182.1	315.4	0.102	5	100.1	488.4	588.5
TR-L M3D (low-density PDN)	0.046 (-45%)	2.3 (+15%)	101.3 (-24%)	151.0 (-17%)	252.3 (-20%)	0.056 (-45%)	5.4 (+8%)	76.8 (-24%)	405.4 (-17%)	482.2 (-18%)
TR-L M3D (high-density PDN)	0.053 (-37%)	2.2 (+10%)	117.3 (-12%)	153.0 (-16%)	270.3 (-15%)	0.065 (-36%)	5.2 (+4%)	87.1 (-13%)	410.3 (-16%)	487.4 (-15%)
S3DC (with PDN)	0.009 (-89%)	1.8 (-10%)	48.0 (-64%)	76.5 (-58%)	124.5 (-63%)	0.010 (-90%)	4.6 (-8%)	38.0 (-62%)	210.0 (-55%)	248.0 (-56%)

limited accessibility to the bot-tier. This results in a low-density PDN design and severe IR-drop in the bot-tier (See Table I). In the improved version of TR-L M3D (with high-density PDN), each 3D cell is designed with larger area to provide additional vertical routing resource for accessing bot-tier’s VDD rails. This enables a high-density and robust PDN design that has low-resistance VSS/VDD delivery paths and solves the IR-drop issue (See Table I). However, enlarging cell area reduces the design density which diminishes its 3D routing benefits. In S3DC, the coaxial routing structure can provide 2x vertical routing capacity compared to the TR-L M3D which uses conventional via-to-metal routing structure. Therefore, S3DC intrinsically supports a robust PDN design (See Table I) without the requirement of requiring additional routing resources. This ensures S3DC can maintain its benefits over 2D after PDN insertion.

We evaluate and compare the 3D benefits of TR-L M3D and S3DC with PDN designs in comparison to 2D CMOS. The results are shown in Table II. In the LDPC benchmark, the TR-L M3D with high-density PDN shows 1.2x total power efficiency and 1.8x density compared to 2D CMOS. Compared to the typical TR-L M3D which only has low-density PDN, though the TR-L M3D with high-density PDN efficiently eliminates the IR-drop issue (See Table I), it has a loss of 25% total power efficiency and 18% density benefits over 2D CMOS. The increased wire power is the main reason for the loss of total power benefit. On the other hand, S3DC shows 2.7x power efficiency and 9x density benefits vs. 2D CMOS while a robust PDN is used and no IR-drop issue is observed (See Table I). In the AES benchmark, the TR-L M3D with high-density PDN has a loss of 16% power and 20% density benefits over 2D compared to the TR-L M3D with low-density PDN. It can be noted the loss of power efficiency is lower in the AES design than in the LDPC design. This is because the AES design is a cell-dominated design where the wire power is a small part of the total power. The increased wire power in TR-L M3D with high-density PDN has less impact on total power in AES design than in LDPC design. For S3DC, it still maintains 2.3x power efficiency, and 9x density over 2D CMOS in AES benchmark. In both AES and LDPC, S3DC has around 10% performance degradation compared with 2D CMOS due to the usage of VGAA transistors, which have a higher-resistivity channel [19]. This disadvantage however, can be overcome in multi-million transistor designs due to significantly shorter wires [20].

## VI. CONCLUSION

In this paper, we study the power-delivery network (PDN) design in Skybridge-3D-CMOS (S3DC) fabric and evaluate the PDN’s IR-Drop and impact on 3D routing. We investigate

and compare it with the PDN design in state-of-the-art monolithic 3D IC and transistor-level monolithic 3D (TR-L M3D). Both low-density and high-density PDN designs in TR-L M3D are evaluated and compared to PDN in S3DC. Due to the improved routing capacity in vertical routing direction, the S3DC can enable a robust PDN design that has negligible IR-drop and also no impact on 3D cell-to-cell density. The evaluation results show that both the TR-L M3D with high-density PDN and S3DC meet the requirement of standard IR-drop budget (<5% VDD) while the TR-L M3D with low-density PDN has severe IR-drop which is out of the IR standard budget. However, the TR-L M3D with high-density PDN has a loss of up-to 25% power efficiency and 20% density benefits over 2D CMOS due to lowering its 3D routing density for robust PDN design while S3DC’s PDN design has no impact on its 3D benefits (up-to 2.7x power efficiency and 9x density compared to 2D).

## REFERENCES

- [1] S. Panth, et al., "Design Challenges and Solutions for Ultra-High-Density Monolithic 3D ICs," *IEEE S3S*, pp. 1-2, 2014.
- [2] J. Cong, et al., "A thermal-driven floorplanning algorithm for 3D ICs," *IEEE ICCAD*, pp. 306-313, 2004.
- [3] J. Shi, et al., "A 14nm FinFET transistor-level 3D partitioning design to enable high-performance and low-cost monolithic 3D IC," *IEDM*, pp. 2.5.1 - 2.5.4, 2016.
- [4] J. Shi, et al., "On the Design of Ultra-High Density 14nm Finfet Based Transistor-Level Monolithic 3D ICs," *IEEE ISVLSI*, pp. 449-454, 2016.
- [5] S. Samal, et al., "Full Chip Impact Study of Power Delivery Network Designs in Monolithic 3D ICs," *IEEE ICCAD*, pp. 565 - 572, 2014.
- [6] Y. Lee, et al., "Ultra High Density Logic Designs Using Transistor-Level Monolithic 3D Integration," *IEEE ICCAD*, pp. 539 - 546, 2012.
- [7] S. Bobba, et al., "CELONCEL: Effective Design Technique for 3-D Monolithic Integration targeting High Performance Integrated Circuits," *IEEE ASP-DAC*, pp. 336-343, 2011.
- [8] M. Li, et al., "Skybridge-3D-CMOS: A Vertically-Composed Fine-Grained 3D CMOS Integrated Circuit Technology," *IEEE ISVLSI*, pp. 403-408, 2016.
- [9] J. Shi, et al., "Routability in 3D IC Design: Monolithic 3D vs. Skybridge 3D CMOS" *IEEE NANOARCH*, pp. 145-150, 2015.
- [10] "Synopsys- Sentauros User Guide," 2015-1.
- [11] "Cadence-Voltus IC Power Integrity User Guide," 2015-8.
- [12] M. Rahman, et al., "Fine-Grained 3-D Integrated Circuit Fabric using Vertical Nanowires," *IEEE 3D-IC*, TS9.3.1 - TS9.3.7, 2015.
- [13] M. Rahman, et al., "Manufacturing Pathway and Experimental Demonstration for Nanoscale Fine-Grained 3-D Integrated Circuit Fabric," *IEEE-NANO*, pp. 1214-1217, 2015.
- [14] J. Shi, et al., "NP-Dynamic Skybridge: A Fine-grained 3D IC Technology with NP-Dynamic Logic", *IEEE TETC*, Vol. PP, Issue. 99, pp. 1-1, 2017.
- [15] A. Veloso, et al., "Challenges and opportunities of vertical FET devices using 3D circuit design layouts," *IEEE S3S*, pp. 1-3, 2016.
- [16] J. Shi, et al., "Architecting NP-Dynamic Skybridge", *NANOARCH*, pp.169 - 174, 2015.
- [17] M. Rahman, et al., "Skybridge: 3-D Integrated Circuit Technology Alternative to CMOS" 2014; <http://arxiv.org/abs/1404.0607>
- [18] Nangate. Nangate 15nm Open Cell Library.
- [19] A. Kranti, et al., "Junctionless nanowire transistor: Properties and design guidelines." *ESSDERC*, pp.357-360, 2010.
- [20] Khasanvis, et al., "Architecting Connectivity for Fine-grained 3-D Vertically Integrated Circuits", *IEEE/ACM NANOARCH*, pp. 175-180, 2015.