Manufacturing Pathway and Experimental Demonstration for Nanoscale Fine-Grained 3-D Integrated Circuit Fabric

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***Abstract*—At Sub-20nm technologies CMOS scaling faces severe challenges primarily due to fundamental device scaling limitations, interconnection overhead and complex manufacturing. Migration to 3-D has been long sought as a possible pathway to continue scaling; however, CMOS's intrinsic requirements are not compatible for fine-grained 3-D integration. In [1], we proposed a truly fine-grained 3-D integrated circuit fabric called Skybridge that solves nanoscale challenges and achieves orders of magnitude benefits over CMOS. In Skybridge, device, circuit, connectivity, thermal management and manufacturing issues are addressed in an integrated 3-D compatible manner. At the core of Skybridge's assembly are uniform vertical nanowires, which are functionalized with architected features for fabric integration. All active components are created primarily using sequential material deposition steps on these nanowires. Lithography and doping are performed prior to any functionalization and their precision requirements are significantly reduced. This paper introduces Skybridge's manufacturing pathway that is developed based on extensive process, device simulations and experimental metrology, and uses established processes. Experimental demonstrations of key process steps are also shown.**

Keywords—3-D Integration; Fine-Grained 3-D Fabric; Vertical Nanowire; 3-D Circuits; 3-D Manufacturing

I. INTRODUCTION

As CMOS is reaching its fundamental limits at nanoscale, fine-grained 3-D CMOS to continue scaling has been extremely difficult to achieve due to inherent doping and customization requirements of CMOS circuits. Partial 3-D attempts with die-die and layer-layer stacking only provide incremental density benefits while retain CMOS scaling challenges, and have their own limitations [2][3]. Skybridge is a new truly fine-grained 3-D integrated fabric that provides an integrated solution for all nanoscale technology aspects, and achieves orders of magnitude benefits [1]. In Skybridge's 3-D integration, uniform vertical nanowires play a key role. Vertical Gate-All-Around (V-GAA) Junctionless transistors that do not require doping variations within the device, are active devices and are realized through material depositions on nanowires. V-GAA Junctionless transistors are interconnected through nanowire connecting Bridges and nanowire surrounding routing structures in a 3-D circuit style that uses only single-type, uniformly sized transistors for logic and memory circuits. Fabric's intrinsic heat management is through heat extraction features and heat dissipating nanowires. Since, formation of all active fabric components is by functionalizing nanowires through material depositions, lithographic precision is required only for nanowire patterning. Moreover, Skybridge's unique circuit design approach with uniform Junctionless transistors ensures doping is required only once during initial wafer preparation, reducing manufacturing constraints further.

In this paper, we highlight Skybridge's manufacturing pathway, and show experimental results. Our experimental demonstrations include high aspect-ratio vertical nanowire patterning and material deposition steps for fabric functionalization. Using direct patterning approach with E-beam lithography, we have demonstrated nanowires with different dimensions; nanowire widths ranging from 197nm to 26nm, and height ranging from 1100nm to 260nm were demonstrated. Using E-beam alignment, exposure and deposition steps we have shown anisotropic material (Ti, Cr for Contact formation) depositions in selective places of the die. For multi-layer pattern definitions and inter-layer material depositions we have developed a technique using over-fill and etch-back method, and shown planarization of both photoresist (PMMA) and interlayer dielectric (SU-8).

The rest of the paper is organized as follows: in Section II we provide an overview of the fabric and discuss its potentials, Section III describes the manufacturing pathway, Section IV shows experimental results, and Section V concludes the paper.

II. SKYBRIDGE FABRIC OVERVIEW

Skybridge design follows a fabric-centric mindset where device, circuit, connectivity, heat management and manufacturing issues are addressed in an integrated manner. Skybridge's core components are key to this mindset. These components are: vertical nanowires, V-GAA Junctionless transistors, Bridges, Coaxial Routing structures, Heat Extraction Junctions, and Heat Dissipating Power Pillars. As mentioned earlier, vertical nanowires (Fig. 1A) are fundamental building blocks, and active component formation on these nanowires is through sequential material depositions. V-GAA Junctionless transistors are stacked on to nanowires, and are interconnected through Bridges and Coaxial Routing structures for functional circuits. V-GAA Junctionless

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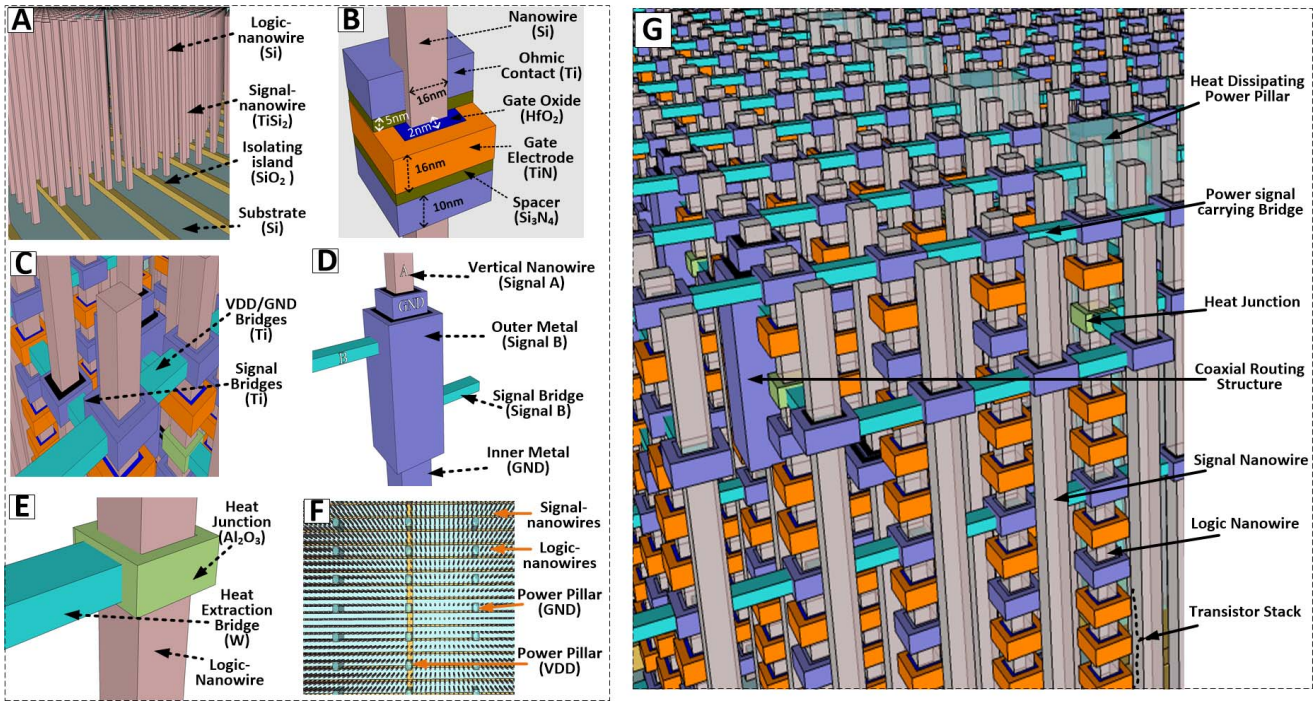

Figure 1. Core components of Skybridge fabric, and abstract fabric representation. A) Arrays of uniform vertical nanowires that serve as template for fabric assembly, B) Vertical Gate-All-Around n-type Junctionless transistor, C) nanowire connecting Bridges, D) Coaxial routing structure for signal propagation and noise shielding, E) Heat Extraction Junction for removal of heat from any nanowire region without interfering with electrical signals, F) large area power and heat extraction pillars in sparse locations, G) Abstract fabric view with all components.

transistors do not require Source/Channel or Channel/Drain doping variations for device operation, and can be formed by stacking materials surrounding nanowires as shown in Fig. 1B. Bridges (Fig. 1C) connect between transistors and contact regions, and are used in conjunction with Coaxial Routing structures (Fig. 1D) for signal propagation in 3-D. Bridges are formed by Tungsten (W) deposition in between nanowires at different layers. Coaxial Routing structures allow multiple signal propagation without interference, and also help in noise mitigation. In these structures, a thick SiO_2 layer provides isolation between two signal carrying regions. For noise mitigation, an extra GND shielding layer is inserted in each Coaxial Routing Structure. Similar to transistor, contact and Bridge formation steps, routing structures are formed through Ti and SiO_2 depositions. Heat Extraction Junction (Fig. 1E) and Heat Dissipating Power Pillars (Fig. 1F) are intrinsic to the fabric and are used for thermal management. These features allow flexibility to be selectively placed in a 3-D circuit layout to control thermal profile without any loss of functionality or performance. Heat Extraction Junctions are thermally conducting, but electrically isolating to ensure logic behavior is not affected. Junction formation is through deposition of Al_2O_3 at selective places of vertical nanowires. Bridges connect to these junctions on one end and to Heat Dissipating Power Pillars on the other, and thus allow heat extraction in 3-D from heated regions in vertical nanowires. These pillars serve the purpose of both power supply (i.e., VDD and GND signals) and heat dissipation. They are large in area (2x2 nanowire pitch), and are sparsely located in the fabric. They have specialized configuration (i.e., silicided pillars and metal fillings) particularly to facilitate heat dissipation. Fig. 1G shows an abstract view of the fabric with all core components.

Following the integrated fabric-centric mindset, Skybridge circuits are designed with only single type uniformly sized transistors. A 3-D dynamic circuit style is used for logic and memory implementations. Due to the unique 3-D integration approach, Skybridge designs achieve tremendous benefits over CMOS. Our analyses reveal for a 4-bit microprocessor, Skybridge design is 30x denser, 2.94x more power efficient and operates at 16% higher frequency in comparison to equivalent CMOS design at 16nm [1]. For a 10million gate based design, interconnect implications were found to be very significant; in the best case interconnection length for the longest wire was 10x shorter, and number of repeaters were reduced by 100x compared to CMOS [4]. Fabric's intrinsic heat extraction features were also found to be very effective in worst case scenarios [6]. Further detail about Skybridge's core architecture, and design aspects can be found in [1][4][6].

III. Skybridge's Manufacturing Pathway

A cross-section of 3-D circuit (3-input 3-D NAND gate) with underlying materials is shown in Fig. 2A. These materials are sequentially deposited on nanowire for Circuit formation. The manufacturing pathway for fabric assembly is derived based on process, device simulations [5] and our experimental demonstration of Junctionless transistor in 2-D [5], and uses existing foundry processes. The process flow, depicted in Fig.

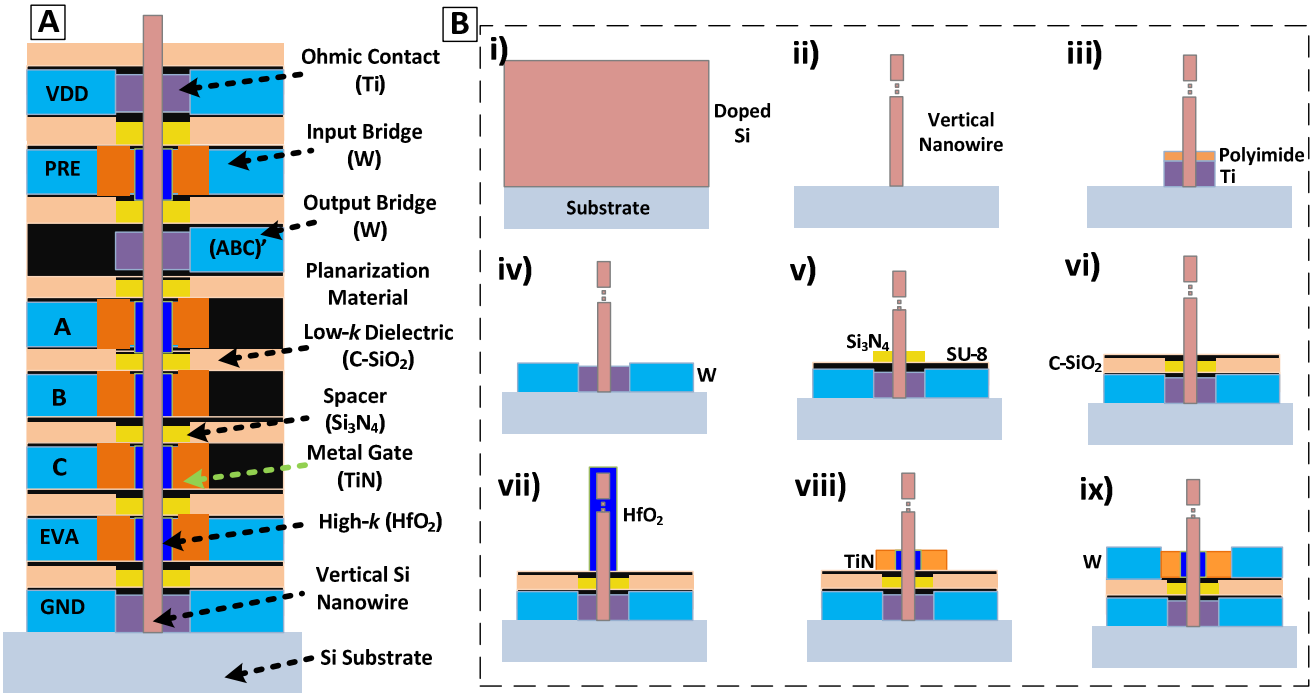

Figure 2. A) Cross-section of a 3-D circuit in Skybridge fabric. B) Key steps for fabric assembly; i) substrate doping, ii) vertical nanowire patterning, iii) anisotropic material (Ti) deposition at the bottom with sacrificial layer, iv) formation of Bridges (W), v) surface planarization with SU-8 and spacer (Si3N4) deposition, vi) low-k inter-layer dielectric (C-SiO2) deposition, and planarization, vii) HfO2ALD deposition, viii) Gate material (TiN) deposition, ix) Gate contact (W) formation.

2B, starts with substrate doping (Fig. 2B(i)), and is followed by nanowire patterning (Fig. 2B(ii)). Subsequent steps involve controlled material depositions on these nanowires. Contact regions are formed through anisotropic metal (Ti) deposition at the bottom with sacrificial layer (Polyimide) on top (Fig. 2B(iii)). The sacrificial layer is used to protect the top region of Contact. This step is followed by metal deposition (W) for interconnect layer (Fig. 2B(iv)), and planarization step with dielectric (SU-8) etch back. Any self-planarizing inter-layer dielectric with low-*k* can be used for surface planarization. It's a two-step process where the dielectric material is overfilled first to cover all substrate features, and then etched back to desired depth. After planarization, spacer (Si_3N_4) material is deposited anisotropically (Fig. 2B(v)). Low-*k* dielectric material (C-doped SiO_2) is deposited next, and is followed by planarization (Fig. 2B(vi)). For transistor's Gate formation, HfO_2 is deposited using ALD (Fig. 2B(vii)), followed by Gate material (TiN) deposition (Fig. 2B(viii)). After TiN deposition, HfO_2 is etched back, and Gate formation is completed by contact material (W) depositions (Fig. 2B(ix)). Similar process steps (Fig. 2B (i-ix)) are repeated for stacking transistors, and to complete fabric assembly.

IV. Experimental Results

We have experimentally demonstrated key steps necessary for Skybridge's assembly. These demonstrations along with Junctionless device validation further prove feasibility of realizing Skybridge fabric.

A. *Formation of Vertical Nanowires*

We have demonstrated high aspect ratio vertical nanowires. Both isolated nanowires and nanowire arrays of different height and width were fabricated. Using E-beam lithography nanowire patterns were defined on positive photoresist (PMMA), and metal deposition was done to be used as hard etch mask. Using these metal etch masks, deep RIE etching was done to form vertical nanowires. An optimized etch recipe was used that had intermediate surface passivation stages. Combination of three gases (SF6, CHF3, and Ar) was used to for etching and surface smoothening, while O_2 was used in interleaved stages for surface passivation. Figs. 3A-B shows vertical nanowire fabrication results. A range of nanowires with different height and width were fabricated. Fig. 3A shows 360nm tall nanowires of different width; smallest width being 26nm on top. Fig. 3B shows nanowire array with each nanowire having 1100nm height and 197nm mostly uniform width. The nanowire width can be further reduced to achieve higher aspect ratios by oxidation and removal techniques similar to the ones presented in [7].

B. *Photoresist Planarization, Alignment and Deposition*

Photoresist planarization is a key step in Skybridge assembly. Spinning a thin layer of photoresist on a substrate with existing high aspect ratio features, usually results in non-uniformities due to surface tension of liquid. The non-uniformities in photoresist layer are detrimental to exposure/writing steps. To overcome this challenge and to

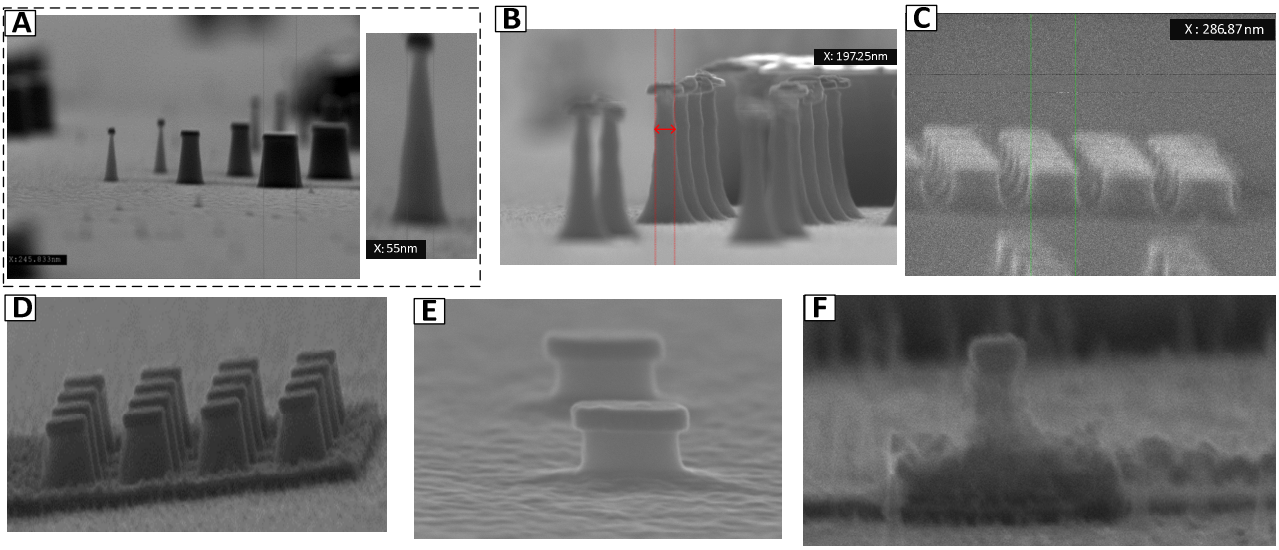

Figure 3. Demonstration of Key Manufacturing Steps for Skybridge Assembly. A) Fabricated nanowire arrays with different dimensions; all the nanowires are 360nm in height, with width ranging from 200nm to 26nm at the top. B) 1100nm tall nanowires with mostly uniform 197nm width. C) After photoresist over-fill and etch-back. D) Demonstration of selective material deposition anisotropically. E) Planarization with SU-8. F) Multi-layer selective depositions.

planarize photoresist layer, we have developed a technique using photoresist over-fill and etch-back. During the over-fill process, several layers of photoresist were coated to completely cover the nanowire features. Subsequently, photoresist was etch-back using an optimized recipe with O_2 plasma to obtain a thin planarized photoresist layer at the bottom of nanowires (Fig. 3C).

After photoresist planarization, E-beam alignment and exposure was done selectively on nanowire surrounding regions to deposit materials for source/drain contact formation. This step was followed by photoresist development, and contact material (Ti) deposition using E-beam evaporator. Fig. 3D shows an example of anisotropic material deposition at selective places of the die.

C. Interlayer Dielectric Deposition and Planarization

Interlayer dielectric provides isolation between electrical components, and is essential in nanofabrication processes. Both self-planarization materials with low-k, and low-k oxides can be used for this purpose. For our experiments, we used SU-8 as self-planarizing interlayer dielectric material. Similar to the photoresist planarization process discussed earlier, SU-8 was overfilled and etched-back to obtain planarized interlayer. SU-8 has self-planarizing capabilities; once the vertical nanowires are covered with SU-8, the top layer planarizes itself. SU-8 is also suitable for our experiments due to its structural rigidity; once hardened, SU-8 is very difficult to remove with wet etchants, and remains unperturbed throughout subsequent processing steps. SU-8 can be hardened both by over-baking and plasma exposure. Fig. 3E demonstrates application of SU-8 as interlayer dielectric.

D. Multi-layer Material Deposition

Following aforementioned steps, and using same set of alignment makers E-beam exposure and deposition can be done to develop multi-layer material stack as shown in Fig. 3F. Similar process steps with controlled etching can be also used for gate-oxide deposition.

V. Conclusion

In this brief, we have introduced Skybridge fabric's manufacturing pathway, and showed recent experimental progress. We have shown key steps necessary for fabric assembly including high aspect-ratio nanowire patterning, photoresist and interlayer dielectric planarizations, and selective multi-layer anisotropic material depositions. Presented work is foundational for experimental realization of fine-grained 3-D integrated circuits fabric, and provides guideline for large-scale assembly.

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