Architecting 3-D Integrated Circuit Fabric with Intrinsic Thermal Management Features

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Abstract— **Migration to 3-D provides a possible pathway for future Integrated Circuits (ICs) beyond 2-D CMOS, which is at the brink of its own fundamental limits. Partial attempts so far for 3-D integration using die to die and layer to layer stacking do not represent true progression, and suffer from their own challenges with lack of intrinsic thermal management being among the major ones. Our proposal for 3-D IC, Skybridge, is a truly fine-grained vertical nanowire based fabric that solves technology scaling challenges, and at the same time achieves orders of magnitude benefits over 2-D CMOS. Key to Skybridge's 3-D integration is the fabric centric mindset, where device, circuit, connectivity, thermal management and manufacturing issues are co-addressed in a 3-D compatible manner. In this paper we present architected fine-grained 3-D thermal management features that are intrinsic components of the fabric and part of circuit design; a key difference with respect to die-die and layer-layer stacking approaches where thermal management considerations are coarse-grained at system level. Our bottom-up evaluation methodology, with simulations at both device and circuit level, shows that in the best case Skybridge's thermal extraction features are very effective in thermal management, reducing temperature of a heated region by up to 92%.**

Keywords—3-D Integrated Circuit; Skybridge; Vertical Nanowire; 3-D Thermal Management; Thermal Modeling

I. INTRODUCTION

Continuing traditional way of IC scaling is becoming very difficult at sub-20nm due to fundamental device scaling limits[1], interconnection bottlenecks [2], and increasing manufacturing complexities [3][4]. Partial 3-D attempts using die-die or layer-layer stacking to continue scaling provides linear density benefits, but retain 2-D CMOS challenges, and add new constraints of their own such as hot-spot formation [4], mechanical stress [4], etc. At nanoscale, confined geometries of transistor channels have drastically reduced thermal conductance [7], which contributes to self-heating. When these nanoscale transistors are detached from the heat-sink in layer-layer and die-die stacking configurations, circuit activities lead to hot-spot developments. Safeguarding approaches such as reducing circuit activity, improving packaging configurations are typically applied to address this issue. However, these approaches might not be sufficient to dissipate heat at ultra-scaled dimensions, or for emerging 3-D fabrics.

Skybridge is a fine-grained 3-D integrated circuit fabric that solves CMOS scaling challenges, and achieves benefits of true 3-D integration; for large-scale designs, evaluation results show orders of magnitude benefits compared to equivalent 2-D CMOS based designs [5]. The fabric design follows an integrated mindset, where architectural and design choices are optimized at physical fabric level for 3-D compatibility. Nanoscale thermal management is preventative, addressed through architectural choices at physical fabric level with heat extraction features being built-in as core fabric components; this is a significant departure from traditional CMOS mindset, where heat extraction from active circuit is reactive and addressed only as after-thought (i.e., during operation, and at system level). Fabric's intrinsic heat extraction features allow heat extraction and dissipation from heated regions within 3-D circuits, and thus prevent hotspot development. These intrinsic features include: (i) Heat Extraction Junctions (HEJs) for extracting heat in the 3-D circuit, (ii) Heat Extraction Bridges (HEBs) for carrying extracted heat, (iii) sparsely placed large area Heat Dissipating Power Pillars (HDPPs) for heat dissipation to sink. Additionally, placement of power rails and contacts in physical layout are also aimed towards minimizing heat.

In this paper, we discuss 3-D thermal management in Skybridge fabric. We present an overview of the fabric, and show core heat extraction features. We present our detailed thermal simulation approach that accounts for nanoscale material properties, heat transport, 3-D circuit operation, 3-D circuit placement and layout. We discuss thermal evaluation results considering worst-case static heat dissipation scenarios to show the effectiveness of fabric's intrinsic heat management features. Our results show Skybridge's heat extraction features are effective in reducing the temperature of a heated region by 92% in the best case; the temperature was reduced from 4307K to operating temperature at 400K for the most heated region. The average temperature of the circuit was reduced by 73%. These results are significant, and pave way for new 3-D circuit design paradigm with intrinsic fine-grained thermal management.

The paper organization is as follows: in Section II we present fabric overview and intrinsic heat extraction features, in Section III we show thermal modeling of 3-D circuit, and present thermal evaluation results in Section IV. Finally, we draw conclusions in Section V.

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II. SKYBRIDGE FABRIC OVERVIEW

Skybridge's architecture relies on six core fabric components that are specifically architected to address 3-D device, circuit, connectivity, thermal management and manufacturing requirements. One of the major components is uniform vertical nanowires (Fig. 1A). These nanowires are building blocks, and all active components for fabric assembly are formed on these nanowires primarily through material deposition techniques. Junctionless transistors (Fig. 1B) that do not require abrupt doping variation within the device are active devices. These devices are stacked on nanowires and are interconnected using Bridges (Fig. 1C) and Coaxial structures (Fig. 1D) to implement logic and memory functionalities. Heat extraction features: Heat Extraction Junction (Fig. 1E), Heat Extraction Bridges (Fig. 1E), and Heat Dissipating Power Pillars (Fig. 1F) are intrinsic to the fabric and are used for thermal management. These features allow flexibility to be selectively placed in a 3-D circuit layout to control thermal profile without any loss of functionality or performance. An abstract view of the fabric with all core components is shown in Fig. 1G. In the following we discuss the roles of Skybridge's intrinsic heat extraction features:

(i) Heat Extraction Junctions (HEJs) (Fig. 1E) are specialized junctions that are used only to extract heat from heated regions in logic implementing nanowires. These junctions are thermally conducting, but electrically isolating to ensure logic behavior is not affected. Junction formation is through deposition of Al_2O_3 at selective places of vertical nanowires. Al_2O_3 has high thermal conductivity (30 $Wm^{-1}K^{-1}$ [9]), and is a well-known insulator. In conjunction with HEBs, these junctions allow heat extraction from any place in the 3-D circuit, and heat dissipation through Heat Dissipating Power Pillars (HDPPs).

(ii) Heat Extraction Bridges (HEBs) (Fig. 1E) connect to HEJs on one end and to HDPPs on the other, and thus allow heat extraction in 3-D from heated regions in vertical nanowires. HEBs are different from other generic signal carrying Bridges, since these always carry only one type of electrical signal (i.e., GND signal) and serve the purpose of heat extraction only.

(iii) Heat Dissipating Power Pillars (HDPPs) serve the purpose of both power supply (i.e., VDD and GND signals) and heat dissipation. These pillars are large in area (2x2 nanowire pitch), and are sparsely located in the fabric. They have specialized configuration (i.e., silicided pillars and metal fillings) particularly to facilitate heat dissipation. The VDD and GND contacts in each logic nanowire connect to these large area pillars through Bridges, and also allow heat transfer to low temperature in the bulk. The power pillars are different in-terms of dimension, layout and material configuration from signal pillars, which carry input/output/clock signals from different logic/clock stages.

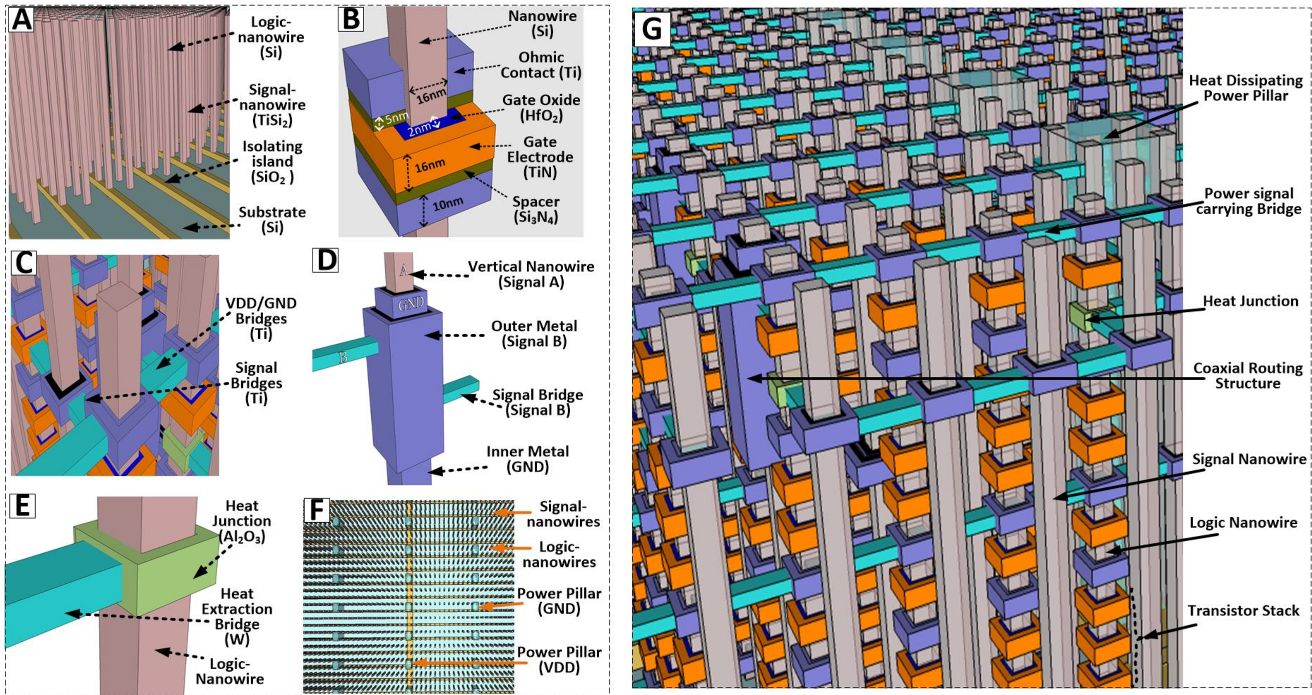

Figure 1. Core components of Skybridge fabric, and abstract fabric representation. A) Arrays of uniform vertical nanowires that serve as template for fabric assembly, B) Vertical Gate-All-Around n-type Junctionless transistor, C) nanowire connecting Bridges, D) Coaxial routing structure for signal propagation and noise shielding, E) Heat Extraction Junction for removal of heat from any nanowire region without interfering with electrical signals, F) large area power and heat extraction pillars in sparse locations, G) Abstract fabric view with all components.

In addition to these intrinsic features, 3-D circuit layouts are also designed to maximize heat dissipation. The power rail contacts in logic carrying nanowires are especially positioned for this purpose. The placement of power rail contacts determine current flow direction, and in turn dictates the heat flow as well; for example, in a vertically implemented dynamic NAND gate if the VDD is placed on the top and GND is placed at the bottom, electrons will flow from GND towards VDD and generate heat along its path, in turn the generated heat will flow from top (i.e., hot region) to bottom (i.e., cool region) towards reference temperature. In Skybridge, the power rails are positioned vertically such that the thermal considerations are taken into account. Since, each logic nanowire pillar accommodates two dynamic NAND gates [5], and one power rail can be shared between two gates, the VDD contact is positioned in the middle and GND contacts are made at the top and at the bottom. This configuration allows heat transfer from VDD to bottom GND and towards heat sink in the bulk and allows the bottom of the nanowires to be in same temperature as the substrate.

In the following sections we present details on thermal characteristics of Skybridge fabric, and show effectiveness of its architectural features (HEJ, HEB and HDPP) in heat removal.

III. Fine-Grained Thermal Modeling of 3-D Circuits

A fine-grained thermal modeling approach was used for thermal profiling of 3-D circuits. The modeling was at transistor level granularity, and accounted for thermal conductivity of materials, nanoscale dimensions, heat transport, circuit operating condition, 3-D circuit placement and 3-D layout. Such fine-grained modeling is important to understand implications of materials, nanoscale confined dimensions, circuit operating conditions, and to judge effectiveness of fabric's intrinsic heat extraction features.

A. Device-level Thermal Modeling

Starting with the modeling of V-GAA Junctionless transistor, we used the electrical analogue [8] of thermal generation described below to estimate temperature gradients.

Approximation of generated heat, Q (Watts) is:

$$Q = Ids * Vds \ldots\ldots\ldots\ldots\ldots (1)$$

where *Ids* is Drain-Source current, and *Vds* is Drain-Source voltage. The relationship between heat (Q) and temperature (T) is:

$$\Delta T = \frac{L}{K * A} * Q \ldots\ldots\ldots\ldots\ldots (2)$$

where L is the heat conduction path's length, k represents thermal conductivity and A is the cross-section area of heat conduction path. Q and T are analogous to current and voltage in electrical domain, thermal resistance is equivalent to electrical resistance. Nanoscale effects and material properties are encapsulated in thermal conductivity parameter K, whereas geometry considerations are taken care in (L/A) portion of eq. (2). At nanoscale, surface scattering, trap states and confinement effects reduce channel conductivity significantly. Pop et al. reported [7] thermal conductivity of 10nm thin silicon layer can be as small as 13 $Wm^{-1}K^{-1}$, which is one order of magnitude less than bulk silicon (147 $Wm^{-1}K^{-1}$). Table 1 lists different materials used in 3-D thermal modeling. Material specifications (i.e., dimensions, thermal conductivity), in the heat flow path are also mentioned in Table 1.

Table 1. Materials, their properties and dimensions

Region	**Material**	**Dimension (L x W x T) nm**	**Thermal Conductivity $Wm^{-1}K^{-1}$**
Drain Electrode	Ti	10 x 16 x 12	21 [10]
Drain-Si	Silicide	10 x 16 x 16	45.9 [11]
Spacer	Si_3N_4	5 x 16 x 18.5	1.5 [12]
Channel	Doped Si	16 x 16 x 16	13 [7]
Gate Oxide	HfO_2	16 x 18 x 2	0.52 [14]
Gate Electrode	TiN	10 x 16 x 6	1.9 [15]
Heat Junction	Al_2O_3	4x16x18.5	30 [9]
Interlayer	C doped SiO_2		0.6 [12]
Bridge	W	43.5x58x 16	167 [16]

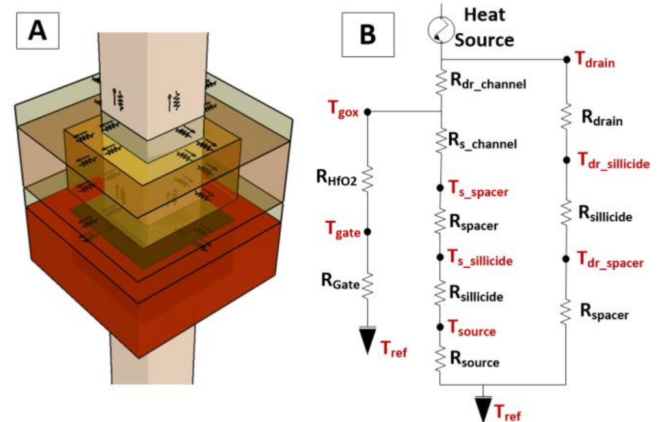

Figure 2. Heat flow direction and thermal resistance network. A) Depiction of thermal resistances, and heat flows in a V-GAA Junctionless transistor, B) Thermal resistance based representation of the transistor.

Using this methodology, V-GAA Junctionless transistor can be represented as thermal resistance network as shown in Fig. 2B; direction of heat path in each transistor region is

shown in Fig. 2A. As shown in Fig. 2A and Fig. 2B, thermal conduction paths to reference temperature are through three contacts at Drain, Gate and Source regions. Transistor's Drain region is the most heated region [7] and acts as heat source in Fig. 2B. From the heat source, heat travels either through the Drain side silicide, spacer and contact, or through the channel towards the Gate contact, or through the channel towards the Source contact. Heat flow is dependent on the lowest resistance path to reference temperature.

B. *Circuit-level Thermal Modeling:*

The methodology described earlier was extended to circuit-level thermal modeling. Physical layout components (V-GAA Junctionless transistor, doped silicon nanowire, Ohmic contact, routing Bridges, interlayer dielectric, signal and power pillars) were modeled with equivalent thermal resistances. Circuit operating conditions (Precharge, Evaluate, or Hold phase [5][6]) were accounted for heat source calculations. Fig. 3A shows physical implementation of circuits that were considered for this work, and Fig. 3B shows equivalent thermal resistance network based representation.

Implementation of two independent 8-input dynamic NAND gates on a single nanowire is shown in Fig. 3A. It also depicts how fabric's intrinsic heat management features are integrated with the circuits; HEJs are placed at outputs of both NAND gates, and HEBs are connected between HEJs and HDDP. In addition to heat dissipation through architected features, heat is also carried though power rails, transistor Gate contacts, doped silicon nanowire, and interlayer dielectric to substrate. To maximize heat dissipation, *GND* connections are placed at both in the top and in the bottom regions of nanowire, and *VDD* connection is made in the middle.

The equivalent 3-D thermal resistance based representation of NAND gates in Fig. 3A is shown in Fig. 3B. Material considerations and dimensions for calculations were according to Table 1. Design rules for nanowire spacing, metal-metal spacing, etc. were taken from [5].

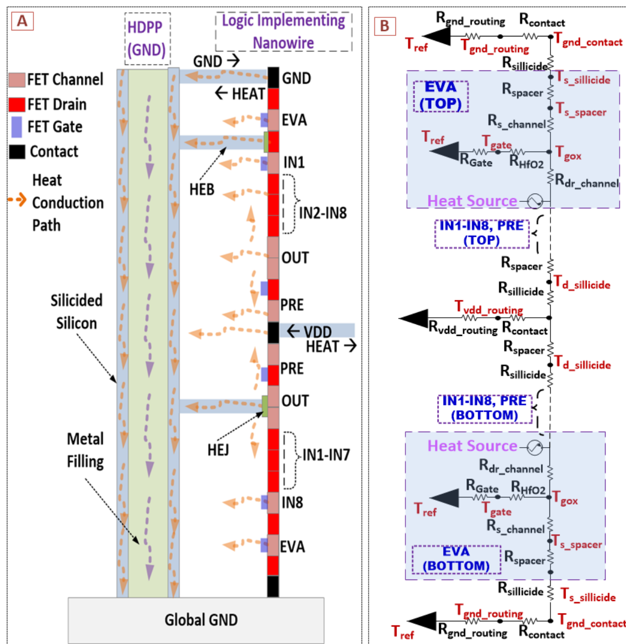

Figure 3. Circuit implementation in physical fabric and equivalent thermal resistance based representation. A) Implementation of two 8-input (In1-In8) NAND gates in a single nanowire is shown. NAND gates follow dynamic circuit style [5] with precharge and evaluate clocking scheme. Integration of heat extraction features, and heat flow directions are also shown. B) Representation of NAND gates using thermal resistances.

IV. Thermal Evaluation Results

We have done extensive simulations to determine thermal gradient of Skybridge circuits under different operating conditions, and to determine effectiveness of intrinsic heat management features. In the following we present thermal simulations of the device and circuits.

A. *Thermal Evaluation of V-GAA Junctionless Transistor*

Fig. 4 shows thermal simulation results obtained using equivalent electrical network simulation in HSPICE for a single isolated transistor. The resistance network model presented earlier, and device characteristics (i.e., *VDD* = 0.8V and *ON* current = 3.2x10^{-5} A) from [5] were used for HSPICE simulations. The reference temperature for all simulations was assumed to be 350K [5], and the routing distance from contact to reference ground was assumed to be very small (i.e., power rails were assumed to be in one nanowire pitch distance) with insignificant thermal resistance.

As shown in Fig. 4A, the temperature is at its peak in the Drain region. As the heat flows towards the channel there are more paths to dissipate through the Drain/Source/Gate contacts; as a result the temperature at the Source side starts to decrease and reaches reference temperature (350K) in the contact. Temperature in Gate-Oxide region is relatively high (400K), due to higher thermal resistance from Gate-Oxide to sink (*GND*).

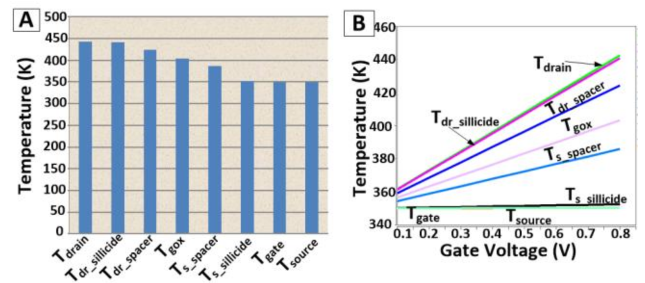

Figure 4. Thermal gradient in V-GAA Junctionless transistor for different bias. A) Temperature profile within the transistor for fixed Gate and Drain voltage (0.8V). B) Temperature profile for voltage sweep (0-0.8V)

The simulation result in Fig. 4A shows the thermal gradient of an isolated transistor with maximum Gate and Drain bias (0.8V) applied. In a practical scenario, Drain voltage can vary depending on circuit's operation; particularly in Skybridge's dynamic circuit style with stacked transistors, Drain-Source voltage of each transistor rarely reaches *VDD*. In order to capture the effect of real operating conditions in 3-D circuits, we carried out simulations for varying Drain voltages (from 0V to 0.8V sweep). The results are shown in Fig. 4B. As shown, the trend in temperature profile is similar to that in Fig. 4A; the temperature is at its maximum in Drain side, and as we move towards the Source or Gate contact regions, temperature decreases and reaches reference temperature. For varying Drain voltages, temperature decrease is linear.

B. Thermal Evaluation of 3-D Circuits

Using the thermal resistance based representation of Skybridge circuits in Fig. 3B, HSPICE simulations were carried out. Simulations were for worst-case static heat generation conditions; during evaluation period with all transistors switched *ON* (i.e., 16 transistors in Fig. 3). Various scenarios were considered for thermal profiling including: (i) without application of any heat extraction features, (ii) with the application of one HEJ, and (iii) two HEJs for whole logic-implementing nanowire. Each of these scenarios was evaluated for different Gate conditions. As mentioned earlier, Gate contacts can contribute to heat extraction, if the Gate temperature is lower than transistor's channel temperature. Gate inputs are driven by output of previous stage; as a result, depending on the operation of previous stage, the temperature in Gate input connection can vary. In our HSPICE simulations, we assumed three different conditions for heat extraction through Gate: (a) no heat extraction (i.e., Gate input temperature is equal to channel temperature), (b) half of maximum heat extraction (i.e., Gate input temperature is half of channel temperature), and (c) maximum heat extraction (i.e., Gate is at reference temperature).

For circuit level simulations, heat sources at Drain side of each transistor was determined by dividing maximum heat (i.e., *ON* current x *VDD*) with number of *ON* transistors. To emulate the conditions of various Gate temperatures, thermal resistances were modeled to allow maximum, half of maximum, and no heat extraction.

Simulation results are shown in Fig. 5; thermal gradient across the logic implementing nanowire (Fig. 3A) is shown. Without the application of heat extraction features, and considering no heat extraction through Gate regions, the temperature reaches up to 4307K. For Gate temperature conditions (b) and (c), when Gate contacts are at half of maximum temperature and at reference temperature respectively, the temperature drops to 667K and 376K respectively.

For scenario (ii), with the application of one HEJ for heat extraction, significant reduction in temperature is observed. In the topmost transistor, temperature drops from 4307K to

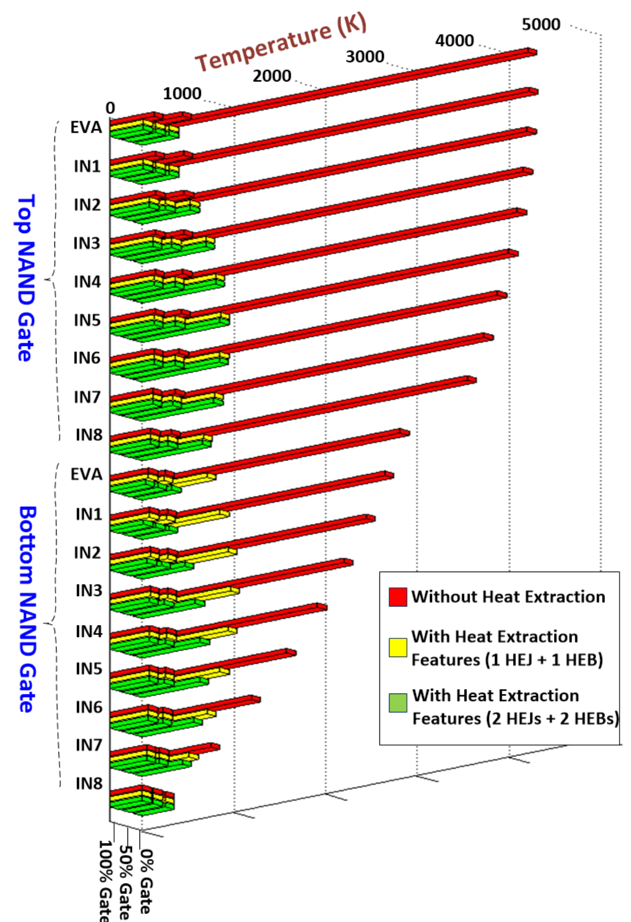

Figure 3. Thermal simulation results show effectiveness of fabric's intrinsic heat extraction features. Two cases are shown: with 1 HEJ and with 2 HEJs per logic nanowire connected to Bridges and HDPPs for heat management. In the case of 2 HEJs per nanowire (Fig. 3), they are connected to two output regions of dynamic NAND gates. In the best case (with 2 HEJs connected, and Gate electrode at reference temperature) the temperature reduction was 90% for the most heated region, and 78% was the average temperature reduction of whole nanowire implementing logic.

400K, 376K and 367K respectively for conditions (a), (b) and (c) respectively. Temperature drop is also observed across other transistors. The average temperature reductions across circuits are 73.3%, 12.2% and 4.8% respectively for conditions (a), (b) and (c).

When 2 HEJs are used for heat extraction (scenario (iii)) from the logic-implementing nanowire, further improvements in thermal profiles are observed. Average temperature reductions are 78.1%, 15.4% and 6.5% respectively for conditions (a), (b) and (c).

These results validate the effectiveness of fabric's heat extraction features. Noticeably, average temperature reductions with 1 and 2 HEJs for conditions (b) and (c) are

well below the breakdown temperature of Junctionless transistors [17]. Depending on design requirements, modifications can be done with placement of HDPPs and number of HEJs in circuits to reduce the average temperature even further.

V. CONCLUSION

In this paper, we detailed a fine-grained approach for heat management in 3-D, and shown its effectiveness through comprehensive modeling and simulations. The modeling approach takes into account material properties, nanoscale effects, 3-D circuit and 3-D layout details. Simulation results, even for a very pessimistic heat source assumptions show that a single Heat Extraction Junction combined with Heat Extraction Bridge and Heat Dissipation Power Pillar can reduce the temperature of a heated region by 92%, and the average temperature of a logic-nanowire as a whole can be reduced by 73%. The fine-grained heat management approach presented in this paper is unique, and presents new opportunities for integrated circuit design with thermal considerations.

REFERENCES

[1] Fischetti, M. V., et al., “Scaling MOSFETs to 10 nm: Coulomb Effects, Source Starvation, and Virtual Source”. International Workshop on Computational Electronics, 2009.

[2] Puri, R. & Kung, D.S., “The dawn of 22nm era: Design and CAD challenges”. International Conference on VLSI. Pp: 429-433, 2010.

[3] Black, B., et al., “Die Stacking (3D) Microarchitecture”. IEEE/ACM International Symposium on Microarchitecture. Pp: 469-479, 2006.

[4] Lau, J.H. “Evolution, challenge, and outlook of TSV, 3D IC integration and 3d silicon integration”. International Symposium on Advanced Packaging Materials. pp: 462-488, 2011.

[5] Rahman, M., Khasanvis, S., Shi, J., Li, M., & Moritz, C. A., “SkyBridge: 3-D Integrated Circuit Technology Alternative to CMOS,” Preprint available at- http://arxiv.org/abs/1404.0607

[6] Rahman, M., Narayanan, P, Khasanvis, S., Nicholson, J. & Moritz, C. A., “Experimental Prototyping of Beyond-CMOS Nanowire Computing Fabrics,” Proceedings of IEEE/ACM International Symposium on Nanoscale Architectures. pp: 134-139, 2013.

[7] Pop, E, “Energy dissipation and transport in nanoscale devices,” Nano Research. vol. 3, pp. 147-169, 2010.

[8] Swahn, B. & Hassoun, S., “Electro-Thermal Analysis of Multi-Fin Devices,” IEEE Transactions on Very Large Scale Integration Systems, vol. **16**, pp. 816-829, 2008.

[9] Dinash. K, Mutharasu, D. & Lee, Y. T., “Paper study on thermal conductivity of Al2O3 thin film of different thicknesses on copper substrate under different contact pressures,” IEEE Symposium on Industrial Electronics and Applications, vol. 620, pp. 25-28, 2011.

[10] Wang, H. & Porter, W. D, “Thermal Conductivity 27: Thermal Expansion 15,” DEStech Publication Inc, 2003.

[11] Neshpor, V.S., “The thermal conductivity of the silicides of transition metals,” Journal of Engineering Physics, vol. 15, pp 750-752, 1968.

[12] Tritt, T. M. “Thermal Conductivity: Theory, Properties, and Applications,” Kluwer Academic, 2004.

[13] Griffin, A. J., Brotzen, F. R. & Loos, P. J., “The effective transverse thermal conductivity of amorphous Si3N4 thin films,” Journal of Applied Physics, vol. 76, pp. 4007-4011, 1994.

[14] Panzer, M. et al., “Thermal Properties of Ultrathin Hafnium Oxide Gate Dielectric Films,” IEEE Electron Device Letters, vol. 30, pp. 1269-1271, 2009.

[15] Pierson, H. O., “Handbook of Refractory Carbides and Nitrides: Properties, Characteristics, Processing, and Applications,” pp. 223-247, Noyes Publications, 1996.

[16] Lu, X., “Thermal conductivity modeling of copper and tungsten damascene structures,” Journal of Applied Physics, vol. 105, pp. 1-12, 2009

[17] Das, S. et al., “Performance of 22 nm Tri-Gate Junctionless Nanowire Transistors at Elevated Temperatures,” ECS Solid State Letters, vol. 2, 2013.