Invited Paper

Heterogeneous integration of epitaxial nanostructures – Strategies and application drivers

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ABSTRACT

In order to sustain the historic progress in information processing, transmission, and storage, concurrent integration of heterogeneous functionality and materials with fine granularity is clearly imperative for the best connectivity, system performance, and density metrics. In this paper, we review recent developments in heterogeneous integration of epitaxial nanostructures for their applications toward our envisioned device-level heterogeneity using computing nanofabrics. We first identify the unmet need for heterogeneous integration in modern nanoelectronics and review state-of-the-art assembly approaches for nanoscale computing fabrics. We also discuss the novel circuit application driver, known as Nanoscale Application Specific Integrated Circuits (NASICs), which promises an overall performance-power-density advantage over CMOS and embeds built-in defect and parameter variation resilience. At the device-level, we propose an innovative cross-nanowire field-effect transistor (xnwFET) structure that simultaneously offers high performance, low parasitics, good electrostatic control, ease-of-manufacturability, and resilience to process variation. In addition, we specify technology requirements for heterogeneous integration and present two wafer-scale strategies. The first strategy is based on *ex situ* assembly and stamping transfer of pre-synthesized epitaxial nanostructures that allows tight control over key nanofabric parameters. The second strategy is based on lithographic definition of epitaxial nanostructures on native substrates followed by their stamping transfer using VLSI foundry processes. Finally, we demonstrate the successful concurrent heterogeneous co-integration of silicon and III-V compound semiconductor epitaxial nanowire arrays onto the same hosting substrate over large area, at multiple locations, with fine granularity, close proximity and high yield.

Keywords: Computing nanofabric, cross-nanowire field-effect transistor, epitaxial nanostructure, heterogeneous integration, semiconductor nanowire, NASICs.

1. INTRODUCTION

1.1 Demand and proposal for heterogeneous integration in nanoelectronics

Speed and energy efficiency, besides manufacturing cost, are the major metrics that have driven the miniaturization of semiconductor electronic devices and circuits for at least the past 4 decades. Constrained by fundamental physics limits, further scaling of the predominantly used silicon (Si)-based field-effect transistors (FET) is becoming increasingly prohibitive. Alternatively, two major research and development directions that have become very popular within the past decade are: i) transport-enhanced channels (*e.g.*, strain-engineered and high-mobility materials) for FET deployment to push the speed limit[1-4], and ii) low dissipation concept devices whose switching mechanism is not limited by thermal diffusion.[5-7] If successful, both research directions can possibly extend scaling or at least delay the problem even further. The maximum benefit of these replacement devices cannot be obtained, however, without a consideration spanning across the material, device, and circuit architecture layers. In particular, their strategic placement and intimate integrations on-chip should be corroboratively developed.

Also within the past decade, an increasingly important yet tangential demand is the heterogeneous integration of hybrid functionalities. Envisioned to be included in the so-called System-in-Package (SiP) are non-digital components such as

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sensors, actuators, passives, and others that would enhance the interactions of nanoelectronics with people and environment.[1] From the technology viewpoint, wafer-to-wafer and die-to-die (*e.g.*, with ~5×5 mm^2 area) bonding are two promising techniques for heterogeneity, especially for System-on-Chip (SoC) applications, yet the achievable integration granularity is mostly medium or coarse.[8-11] The wafer-level bonding approach is also commonly known as three-dimensional (3-D) integration technology.[12-13] Monolithic epitaxial growth on multi-layered substrates is another contending technology with demonstrated success.[14] However, the degree of heterogeneity is rather limited and the demand of growing high-quality epitaxial layers *in-situ* remains high. Moreover, epitaxial layer printing has yielded among the best integrated device and circuit performance[15] yet it also suffers from a limited degree of heterogeneity. Conversely, finer granularity heterogeneous integration has been demonstrated only with similar technology such as embedding flash memory into microprocessors.[16]

In order to sustain the historic progress in information processing, transmission, and storage, concurrent integration of heterogeneous functionality (*e.g.*, very high performance or ultralow power switching, short-term storage, signal routing, *etc.*) and materials (*e.g.*, high-mobility semiconductor channels, charge-based storage dielectrics, capacitance-based storage polymers, *etc.*) with scalable proximity is clearly imperative for the best connectivity, system performance, and density metrics. A truly versatile heterogeneous integration technology should permit fine granularity, high-degree of heterogeneity, wafer-size scalability, and minimal intrinsic performance degradation post-integration.

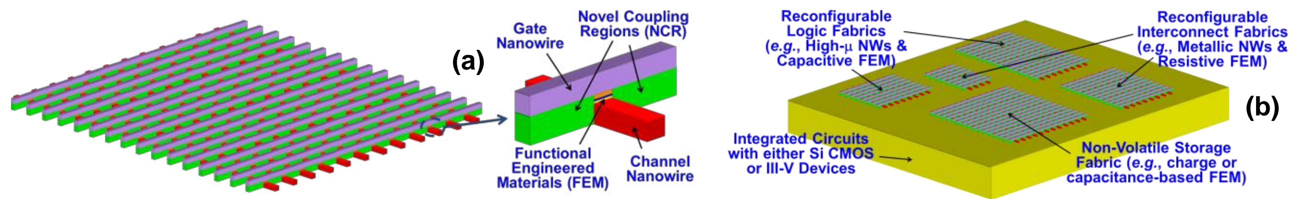

Figure 1. (a) Schematics of the proposed nanoelectronic computing fabric and innovative cross-point devices, named xnwFET. (b) Illustration of fine-granularity and post back-end-of-line (BEOL) integration of various nanofabrics above a pre-fabricated integrated circuits chip.

We envision introducing such heterogeneity to integrated nanoelectronics at the device-level through cross-layer innovation and using computing nanofabrics.[17-25] A nanofabric is composed of orthogonal semiconductor or metal nanowire grids, functional engineered materials (FEM) sandwiched in between, and the resultant cross-point devices (Fig. 1(a)). Above the surface of a pre-fabricated custom design integrated circuit (IC) (*e.g.*, with either Si CMOS or III-V compound semiconductor devices) with partial metallization, nanofabrics with wide range of functionality are concurrently attached with fine granularity (Fig. 1(b)). Constructed with different constituent nanowires and FEM, the nanofabrics can perform reconfigurable logic computations, non-volatile storage, reconfigurable signal routing, and other functions. The ends of the nanowires in each nanofabric are aligned to the metal pin pads patterned atop the underlying IC. The input and output signals of each computing nanofabric, as well as any reconfiguration control biasing signals, are thus provided by the built-in circuitry in the hosting IC.

1.2 Review of the state-of-the-art computing fabric assembly approaches

Before establishing the strategy for device-level heterogeneous integration toward the aforementioned computing nanofabric deployment, we first review state-of-the-art techniques for aligned quasi-one-dimensional (quasi-1-D) epitaxial nanostructure formation. We have previously categorized them and evaluated their strengths and limitations[26]. These are summarized below:

(a) *In situ* aligned growth: nanowires or nanotubes are simultaneously aligned while they are being synthesized on a target substrate. Alignment during growth is typically achieved using some form of guiding. Representative techniques include substrate or template guiding,[27-28] electric field guiding,[29-30] and gas flow guiding.[31-32] While arrays containing more or less parallel nanowires or nanotubes could be demonstrated, the desired control over key parameters such as array pitch/diameter could not be achieved. The control of pitch and diameter depends on catalyst engineering, since nanowire synthesis often relies on catalytic processes. The alignment challenge thus hinges on the ability to form a nanoscale periodic array of catalyst nanoparticles (*e.g.*, as a straight dotted line) whose diameter distribution should be narrow. In addition, the catalyst material compatibility with the substrate and the thermal budget involved in the nanowire or nanotube synthesis are two major technological limitations for the *in situ* techniques.

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(b) *Ex situ* aligned assembly: nanowires or nanotubes are first synthesized elsewhere (through techniques such as vapor-liquid-solid (VLS) growth) and then assembled onto the target substrate. Representative techniques include the Langmuir-Blodgett technique,[33-34] fluidic-guided method,[35] electric field directed assembly,[36-38] organic self-assembly,[39-40] and stamping transfer.[41-45] While nearly parallel nanowire or nanotube arrays have been fabricated, these methods permit no control over the precise assembly locations as well as array pitch/diameter. The critical challenge is therefore to attach each nanowire or nanotube onto a precise position on the substrate surface and in the right orientation. This in turn rests on the feasibility of preparing a periodic line array with nanoscale pitch and linewidth on the substrate surface, a process which can obtain substantial leverage on the advances in lithography. Compared with *in situ* approaches, *ex situ* techniques offer a much wider variety of material choices and synthesis processes owing to the ultra-low thermal budget involved. In addition, a tighter distribution of nanowire/nanotube diameters is allowed, as the source nanowire or nanotube materials could be purified prior to the assembly process.

(c) Nanolithography-based patterning and etching: the usually crystalline semiconductor material layer pre-synthesized on the target substrate surface is first patterned by nanolithography and then anisotropically etched to create a periodic nanowire array. While the etching process is rather standard, there are two very promising nanoscale patterning techniques: nanoimprint lithography (NIL)[46] and superlattice nanowire pattern transfer (SNAP).[47-48] These approaches in principle meet the nanowire pitch and number criteria, yet they possess some subtle practicality concerns. Since the sidewall surfaces of these nanowires are usually damaged during the etching process, caution should be exercised to prevent significant degradation of the resultant device performance. Also, the choice of semiconductor nanowire material is more limited compared with either the *in situ* or *ex situ* approach.

Although many pioneering contributions have been made by the techniques summarized above, there remain several areas for improvement. For instance, some rely on advanced and expensive fabrication processes such as NIL and superlattice epitaxy, which have not been used in mainstream production facilities. In addition, many chemical self-assembly and field-directed methods could only cover a localized wafer footprint. Even if these nanotechnologies might possibly be scaled up to cover the entire wafer, wafer-scale precision control as demanded by low-cost, high-yield manufacturing would be deemed very difficult if not impossible. The most promising pathway, among others, is the hybrid top-down/bottom-up directed self-assembly (DSA) approach that is however compromised by its low throughput, inaccurate registration, and limited density.[1]

2. APPLICATION DRIVERS

2.1 Nanoscale application specific integrated circuits

We have previously proposed a novel nanofabric concept called Nanoscale Application Specific Integrated Circuits (NASICs), which is a semiconductor nanowire grid-based computing fabric targeted as a CMOS replacement technology.[17,21,49-50] NASICs rely on 2D grids of semiconductor nanowires, with cross-nanowire field-effect transistors (xnwFET) at certain cross-points, that utilize computational streaming supported from CMOS. A fabric-centric mindset or integrated approach across devices, circuit style, manufacturing techniques and architectures is followed, with design choices and optimizations at individual levels made compatible with the fabric as a whole. This mindset is anchored in a belief that at nanoscale the underlying fabric, rather than the device alone, is how significant progress could be made in system-level capabilities. This is in direct contrast to 'device-first' approaches that focus on MOSFET-replacement devices essentially preserving the CMOS circuit styles and manufacturing paradigms for interconnect intact.

Fig. 2(a) shows a 1-bit full adder implemented on the NASIC fabric. This includes a semiconductor nanowire grid with peripheral microwires that carry VDD, VSS and dynamic control signals. xnwFETs are shown at certain cross-points in the diagram and all of them are identical with no arbitrary doping or sizing requirement. Customization of the grid is limited to defining the positions of xnwFET. Furthermore, NASICs use a single doping type in all xnwFETs to reduce manufacturing requirements and improve performance.[50] Channels of xnwFETs (blue regions) are oriented horizontally on the left plane, and vertically on the right. Inputs are received from vertical nanowires in the left plane. These act as gates to horizontal xnwFETs implementing one stage of a dynamic circuit. The output of horizontal nanowires acts as gate to the next set of xnwFETs whose channels are aligned in the vertical direction (right NAND plane). Multiple such

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NASIC tiles can be cascaded together to form more complex circuitry such as microprocessors[51] and image processing systems.[52]

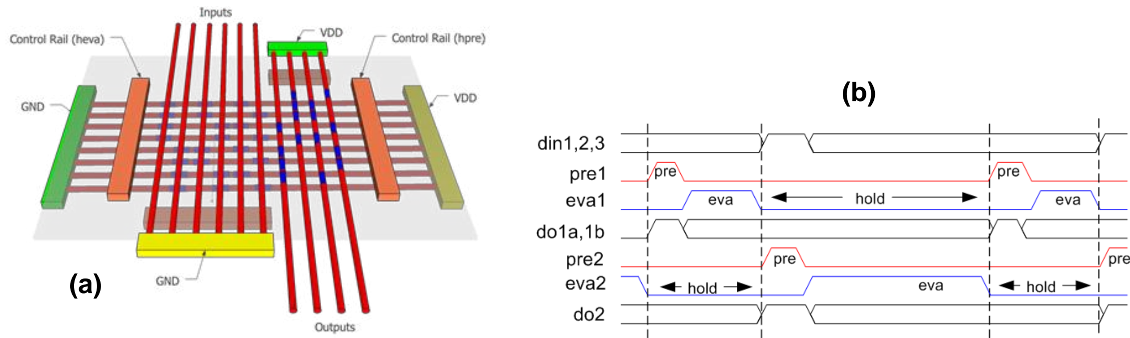

Figure 2. (a) Schematics of the 1-bit NASIC adder. (b) The 3-phase timing scheme for NASICs.[21]

NASICs use a dynamic circuit style with control signals driven from external reliable CMOS circuitry. Control signals coordinate the flow of data through NASIC tiles: horizontal and vertical signals are different, supporting cascading. Fig. 2(b) shows a typical NASIC control scheme but other schemes are also possible. Horizontal nanowire outputs are initially pre-charged to logic '1' by asserting *pre1*. *pre1* is then switched off and *eva1* is asserted to evaluate inputs. Vertical nanowires are simultaneously pre-charged (*pre2* is asserted). In the next phase, both *pre1* and *eva1* are switched off, and the horizontal nanowires are in 'hold' phase, during which time *eva2* is asserted and outputs from the tile are evaluated. The hold phase implements implicit latching of the nanowire output after evaluation without the need for expensive flip-flops, and is essential for cascading multiple nanowire stages. Subsequent stages are evaluated using similar cascaded clocking schemes (*pre3* and *eva3*).

More recently N^3ASICs, a variant on the NASIC fabric was proposed and evaluated.[23,53] The N^3ASICs fabric supports 3D integration with CMOS metal stacks and relaxes overlay precision requirements compared to equivalent scaled CMOS fabrics. Work on NASICs has also spurred research into other emerging nanofabrics based on graphene[54-55] and spin.[56-57] Readers are referred to Refs. 17 and 21 for more details about NASIC.

2.2 Generic cross-nanowire field-effect transistor and performance modeling

Cross-nanowire field-effect transistor (xnwFET) consists of two orthogonal nanowires separated by a dielectric;[58] one nanowire acts as gate and the other as channel (Fig. 3(a)). It is noted that both rectangular and cylindrical nanowire cross-sections are possible depending on the performance target as well as the manufacturing or synthesis process used. In this device, the gate, source, drain, and substrate regions are all doped n^+ (~10^{20} dopants/cm^3) to reduce series and contact resistances and the channel is doped *p*-type without losing generality. This xnwFET is an inversion mode (IM) device similar to conventional MOSFETs: applying a positive voltage at the gate terminal inverts the *p*-doped channel to generate mobile electrons leading to *n*-type FET behavior.

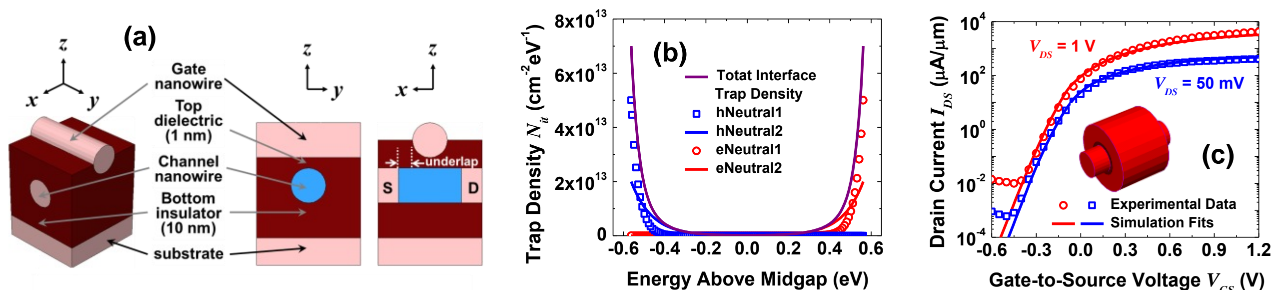

Figure 3. (a) A generic xnwFET structure. (b) Calibrated Si/oxide interface trap density. (c) Validation of the calibrated simulations against experimental data extracted from a gate-all-around nwFET.[59]

For xnwFET performance estimation and design optimization, we have performed technology computer-aided design (TCAD) simulations using Synopsys® Sentaurus Device.[17-18,20-21,24-25] To ensure modeling accuracy, we have first calibrated key model parameters against experimental data. Although credible data extracted from the exact same

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experimental structure are unavailable, we have chosen data from nwFET (not xnwFET) devices at similar dimensions[59-63] for our calibration endeavors. The three key sets of calibrated parameters are:

(a) Mobility degradation at interfaces: during MOSFET operation, the high transverse electric field forces strong interaction between the Si/oxide interface and the mobile charges. These mobile charges will then experience scattering events due to acoustic surface phonons as well as surface roughness. The Enhanced Lombardi Model option within the Enormal option to Mobility captures these two effects and degrades the mobile charge mobility accordingly. Respectively for electrons and holes, the calibrated A values are 2.28 and 2.28; the calibrated B values are 4.75×10^5 and 9.93×10^4; the calibrated C values are 28.0 and 94.7. All other parameters assume default values.

(b) Carrier velocity saturation at high field: as the horizontal electric field increases, the carrier drift velocity starts saturating to a finite value denoted as v_{sat}. The Canali model within the HighFieldSaturation option to Mobility captures this effect. The calibrated beta0 values are 3.109 and 3.213 respectively for electrons and holes. All other parameters assume default values.

(c) Interface trap density: the Si crystalline structure terminates at the Si/oxide interface, which introduces localized states with energies within the forbidden gap. These interface states would degrade the MOSFET subthreshold swing, which can be modeled as an extra capacitance C_{it} in parallel with the Si depletion capacitance C_D. Fig. 3(b) shows the calibrated interface trap density exponential distributions within the bandgap.

Before utilizing these calibrated model parameters in our xnwFET simulations, we have first validated their accuracy against experimental device data. The chosen device is a gate-all-around (GAA) nwFET with 15 nm wide Si nanowire diameter, 2 nm thick silicon dioxide (SiO_2) gate insulator, 10 nm thick polysilicon gate electrode layer, and 30 nm long channel length[59] (Fig. 3(c) inset), owing to its similarity with xnwFET. Taking advantage of the cylindrical symmetry, we have first performed the more computationally efficient two-dimensional (2-D) simulations and then refined the results using full 3-D simulations. As depicted in Fig. 3(c), we have validated that TCAD simulations employing the above calibrated model parameters can successfully reproduce the experimental xnwFET data. It is noted that our simulations do not capture the gate-induced-drain-leakage (GIDL) effect at low gate-to-source voltage V_{GS} since that biasing range is untapped in our circuit operations.

Generally speaking, the electric field coupling from the gate nanowire to the channel nanowire in xnwFET is inherently weak for the following reasons:

(a) The contact area through the top dielectric at the nanowire cross-point is infinitesimally small. Especially for the cylindrical structure, the closest contact is made only at the very center of the cross-point owing to the surface curvature in both gate and channel nanowires.

(b) The device channel length, *i.e.*, the gate nanowire width, is roughly the same as the device channel thickness, *i.e.*, the channel nanowire width.

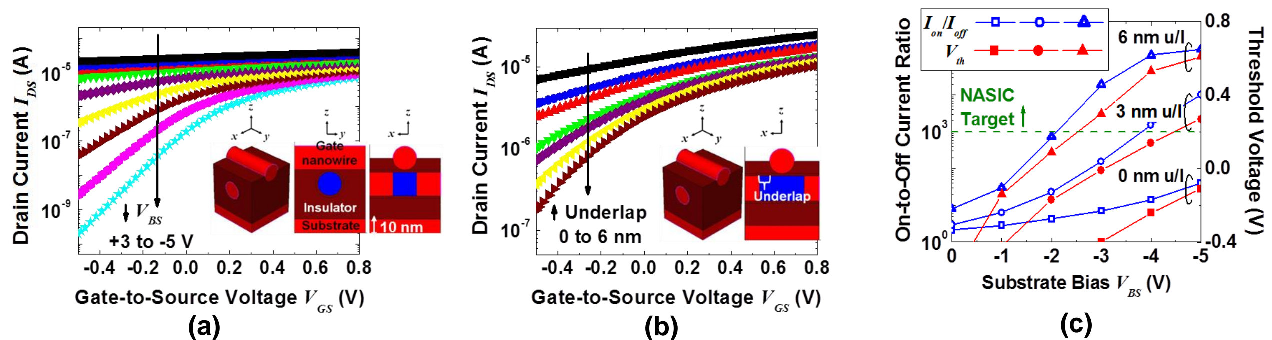

Figure 4. Simulated xnwFET transfer characteristics with different (a) substrate bias and (b) source-drain junction underlap distance. (c) On-to-off state current ratio and threshold voltage optimization with substrate bias and source-drain junction underlap.

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Since poor electrostatic gate-to-channel coupling often compromises the xnwFET integrity as a switching device for circuit implementation, its improvement is mandated through technology-aware explorations of device design and optimization.[17-18,21,24-25] Because all nanowire-level measures (*i.e.*, doping, sizing, and geometry) could not satisfy the xnwFET on-to-off state current ratio (I_{on}/I_{off}) and threshold voltage (V_{th}) requirements at the circuit level,[17] two device-level approaches were additionally considered. The first was to apply a negative substrate bias (V_{BS}) through the bottom insulator to increase both I_{on}/I_{off} and V_{th} of the xnwFET (Fig. 4(a)). This can be attributed to an effective channel doping concentration increase via electrostatic induction by the substrate bias. The resultant reduced short-channel effects simultaneously improve both key design parameters and overall device integrity. The second device-level approach was the introduction of an underlap region between the gate nanowire edge and the source-drain junction (Fig. 4(b) inset). After doing so, the effective channel length would be larger than the gate nanowire width (or gate length) such that an enhanced channel length-to-thickness ratio becomes apparent. Consequently, suppressed short-channel effects were similarly obtained to improve both the I_{on}/I_{off} and V_{th} metrics as confirmed in Fig. 4(b).

Even though the combination of both approaches has revealed great promise for the NASIC computing fabric (Fig. 4(c)),[17] it cannot be applied to the presented heterogeneous integration scheme (Fig. 1) for the following reasons. First, the necessary substrate bias cannot be individually adjusted and applied to each xnwFET within a single fabric because that will in turn overload the underlying IC and thus offset any potential benefit. Second, the precise source-drain junction engineering is very demanding both in terms of dopant introduction and subsequent incorporation via either diffusion or substitution. For example, ultralow energy ion implantation, high-temperature annealing (albeit very short duration), and other manufacturing steps are increasingly challenging especially in the presence of heterogeneous materials and fabrics with a wide range of thermal stability.

2.3 Innovative cross-nanowire field-effect transistor

Overcoming the limitations of the generic xnwFET, we have proposed an innovative xnwFET concept[20-22,24-25] deployable by the envisioned heterogeneous nanofabrics (Fig. 1). The basic device structure has self-aligned FEM at the cross-point and novel coupling regions (NCR) underneath the gate nanowire. It simultaneously offers high performance, low parasitics, good electrostatic control, ease-of-manufacturability, and resilience to processing variation.

The xnwFET gate nanowire can be made of metal or heavily-doped semiconductor to reduce resistance and the channel nanowire is composed of optimally doped high-mobility semiconductor. Several novel and benign features of this structure include:

(a) In contrast to the generic xnwFET, NCR are locally inserted and self-aligned to the top gate nanowire (Fig. 1). After doing so, the gate electric field coupling is no longer limited to across the infinitesimally small cross-point area. Such coupling can now be selectively enhanced via NCR to cover also the channel nanowire sidewalls (right underneath the gate nanowire) yet without incurring a penalty of increased gate-to-source or drain capacitances. This feature is attractive and mandatory for incorporating novel FEM that are usually 'thick'.

(b) Compared to the state-of-the-art non-planar channel transistor which gate electrode wraps around the channel with an Ω-shape to assure good integrity, the straight and flat gate nanowire in the proposed xnwFET structure also permits an innate $4F^2$ cell size while maintaining the needed channel control.

(c) The channel semiconductor nanowire has uniform and heavy doping for accumulation-depletion mode (ADM) operation (versus inversion-mode for xnwFETs) with low on-state resistance. This junctionless (JL) channel scheme eliminates the need to perform dopant implantation and activation anneals in progressively smaller source and drain nanowire volumes; the associated defect annihilation and re-crystallization is already very challenging at present. Also, the control over doping junction abruptness is not necessary. Moreover, the stringent thermal stability requirement on the FEM is instantly relaxed. ADM operation with a respectable subthreshold swing and short-channel control should be fundamentally feasible given tighter electrostatic control enabled by NCR and small channel volumes. Some of these advantages have in fact been observed in the numerous blooming research on JL transistors.[22,64-68]

(d) According to the performance targets, semiconductor channel nanowires with a wide range of low-field mobility or carrier transport ballisticity specifications[3-4,69-80] can be employed in the intrinsically short-channel xnwFET. Although in general the carrier mobility inversely scales with the semiconductor bandgap, the presented xnwFET structure can help to mitigate any associated leakage.

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In validating the effectiveness of NCR and the novel xnwFET, we have performed numerous 3-D TCAD simulations. Since any quantum confinement induced V_{th} shift is absent in the nanowire width of interest,[81] the device electrostatic behavior can be accurately accounted for by the simulator. We have analyzed both generic and novel xnwFETs and extracted their transfer characteristics. Shown in Fig. 5(a) are data for xnwFET with cylindrical nanowires, which confirm that the novel xnwFET with built-in high-permittivity (high-κ) NCR offers substantial improvements in device subthreshold swing, I_{on}/I_{off}, and on-state current (I_{on}) over the generic xnwFET.

To gain further insight into device operation, we have examined the dynamic spatial carrier distribution inside the channel nanowire when the gate nanowire voltage (V_{GS}) was ramped up from the depletion biasing (*e.g.*, -4 V) to accumulation (*e.g.*, 4 V). xnwFET with rectangular nanowires were chosen in this case without losing generality. As evident in Fig. 5(b), the spatial carrier distributions for both devices are the same and rather uniform at V_{GS} = -4 V (or off-state). When V_{GS} is increased (*e.g.*, to 0.4 V), the channel nanowire top surface accumulates more strongly than the two sidewall surfaces; also, the 'accumulation rate' is slightly faster in the novel xnwFET. When V_{GS} is further ramped up (*e.g.*, to 2-4 V), the two channel nanowire sidewall surfaces of the novel xnwFET accumulate as strongly as the top surface; while the two sidewall surfaces of the generic xnwFET do not completely accumulate. Since the observed 'accumulation rate' directly correlates to the device subthreshold swing, the efficacy of the NCR to improve gate electrostatic coupling to the channel nanowire is considered proven (see also Fig. 5(a)). The higher total channel carrier density at V_{GS} = 4 V for the novel xnwFET also explains its high I_{on} and thus I_{on}/I_{off}.

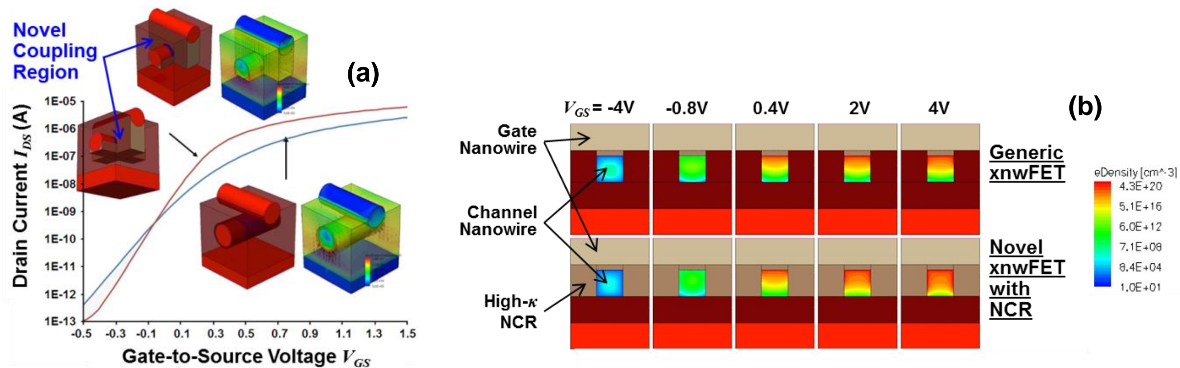

Figure 5. (a) Simulated transfer characteristics of the generic (blue) and novel (red) xnwFETs with cylindrical Si nanowires. Insets show the simulation structures and internal electric field profiles. (b) Simulated carrier concentrations inside the rectangular Si channel nanowire with varying gate nanowire voltage from biasing the channel into depletion (or subthreshold) to accumulation (or on-state).

3. EPITAXIAL NANOSTRUCTURE HETEROGENEOUS INTEGRATION STRATEGIES

3.1 Heterogeneous integration technology requirements

Toward constructing the constituent quasi-1-D epitaxial nanostructures, *i.e.*, nanowire arrays, for the aforementioned computing nanofabrics, any proposed technology should guarantee intrinsic and concurrent control over three key parameters that benchmark the arrays: (i) number of nanowires, (ii) inter-nanowire pitch, and (iii) nanowire diameter.[26] Moreover, a viable heterogeneous integration technology should also be VLSI-compatible and scalable to any substrate size. This is a stringent yet essential requirement not only from manufacturing throughput and robustness considerations; it also constitutes good leverage of the infrastructural investment made by the industry during the past few decades. Furthermore, the technology should possess material selection flexibility, low-thermal budget back-end-of-line (BEOL) compatibility, low-level of cross-contamination, reasonable device-level alignment accuracy against the underlying IC, and minimal perturbation to state-of-the-art foundry processes.

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3.2 Scalable and controlled *ex situ* aligned assembly

Our first strategy for heterogeneous integration of epitaxial semiconductor nanowires is primarily based on the *ex situ* assembly route and subsequent stamping transfer. In contrast to the existing techniques, we have previously proposed and demonstrated a novel concept to combine top-down lithography and crystallographic etching for aligned quasi-1-D nanostructures manufacturing[26]. The baseline strategy comprises three major steps:

(a) Creation of an intrinsically controlled nanoscale periodic line array above the substrate surface

(b) Selective conjugation of quasi-1-D nanostructures only onto the lines within the array

(c) Transfer of the aligned nanostructure array to a different substrate

As detailed in Ref. 26, one possible manifestation of the proposed heterogeneous integration strategy is illustrated in Fig. 6. The first step is to create a nanoscale line array on the substrate surface with a controlled number of lines, pitch, and linewidth. The number of lines and pitch can be defined by standard lithography (Fig. 6(a)) that arguably offers the ultimate intrinsic control for device/circuit designers and requires minimal alteration of the existing layout design infrastructure. Even though state-of-the-art lithography such as extreme ultraviolet (EUV) lithography might be capable of meeting the pitch requirement, a sub-lithographic pitch could indeed be achieved using the spacer double patterning technique.[1] Besides being a cost-effective way to manufacture the necessary nanoscale pitch from a coarse-pitch line array, this approach also permits alignment to pre-existing features on the substrate as a side benefit if necessary.

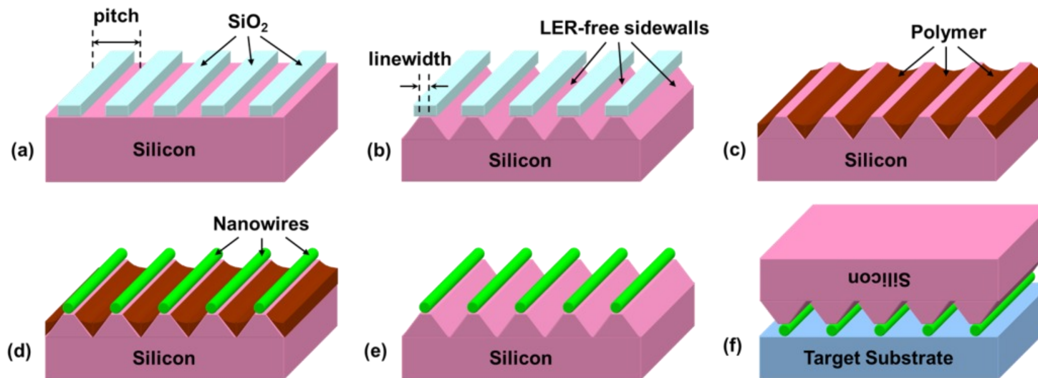

Figure 6. Key manufacturing steps of the proposed nanowire array aligned assembly approach with intrinsic control.[26] (a)-(c) Formation of a nanoscale line array on the assembling substrate with periodically dissimilar surface properties. (d)-(e) Conjugation of the aligned nanowires at the ridge of the LER-free triangular features. (f) Transfer of the aligned nanowire array onto the target substrate surface.

The nanoscale and usually sub-lithographic linewidth can be controlled by using crystallographic etching (Fig. 6(b)) to be larger than, similar to, or smaller than the target nanowire diameter. Contrary to a generic isotropic wet etching, this novel use of crystallographic etching has several advantages. The first salient feature is the creation of a perfect Si line array with atomically straightened line edges even though the masking SiO_2 ribbons atop possess line edge roughness (LER) inherited from the lithography and etching processes. Being a breakthrough by itself, this LER elimination technique truly enables extreme linewidth scaling with suppressed variations that is unparalleled even with the best known fabrication methods. The second feature is very good control over the resultant Si linewidth as determined by the etching time of the slowest etching crystal plane. The third one is the creation of precise and repeatable sidewall profiles (Fig. 6(b)) for subsequent filling of the inter-space; for example, a material with surface properties different from Si such as polymer can be used to fill the inter-space to form a resultant surface with periodically dissimilar properties (Fig. 6(c)).

The second step of our integration strategy involves selective attachment of nanowires only onto the exposed Si line array on the substrate surface, *i.e.*, onto the ridge of the Si triangles (Figs. 6(c)-(d)) but not onto the inter-space polymer (Fig. 6(d)). This can be achieved by manipulating the surface chemistry of the nanoscale substrate lines as well as that of the to-be-assembled nanowires. In other words, the nanowire surface should be attractive to the substrate lines but repulsive to the surface of the interspace polymer or another nanowire. This desired selectivity could come from either an electrostatic interaction or a hydrophobic–hydrophilic interaction, after which the inter-space polymer would be removed without meddling with the assembled nanowire array (Fig. 6(e)). This crucial step could in fact serve as a lift-

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off process to remove any nanowire that might have randomly adsorbed on the polymer surface, a process that can minimize defects in the resultant array and thus greatly enhance manufacturing yield. The last step of our formation strategy is the transfer of the aligned nanowire array onto the target substrate surface (Fig. 6(f)), which is readily accomplished with either the wafer manufacturing bonding process or the established stamping transfer process with slight modifications. The key requirement in this step is accurate alignment between the Si substrate and target substrate, which could be achieved using a crystallographic alignment mark etched into the Si substrate.

To demonstrate the feasibility of the proposed heterogeneous integration strategy, we have performed the following modular experiments toward the formation of aligned Si nanowire arrays.[26] Starting with a (100) surface-oriented Si wafer with a primary flat along the [110] direction, an SiO_2 layer was thermally grown on the surface and then lithographically patterned to form an array of SiO_2 strips as required in Fig. 6(a). Through the SiO_2 openings, the exposed Si was etched in tetramethylammonium hydroxide (TMAH) solution. Since the etching rate is the slowest on the {111} crystal planes, a periodic Si triangular array could thus be obtained (Fig. 7(a)) as required in Fig. 6(b). The SiO_2 strip array was then removed and the Si surface were lightly oxidized (Fig. 7(b)). Polymer material such as poly (methyl methacrylate) (PMMA) was then spin-coated on the substrate surface, followed by an optional reflow and/or etch-back process to form the desired surface with periodic nanoscale Si ridges in between polymer (Fig. 7(c)) as required in Fig. 6(c).

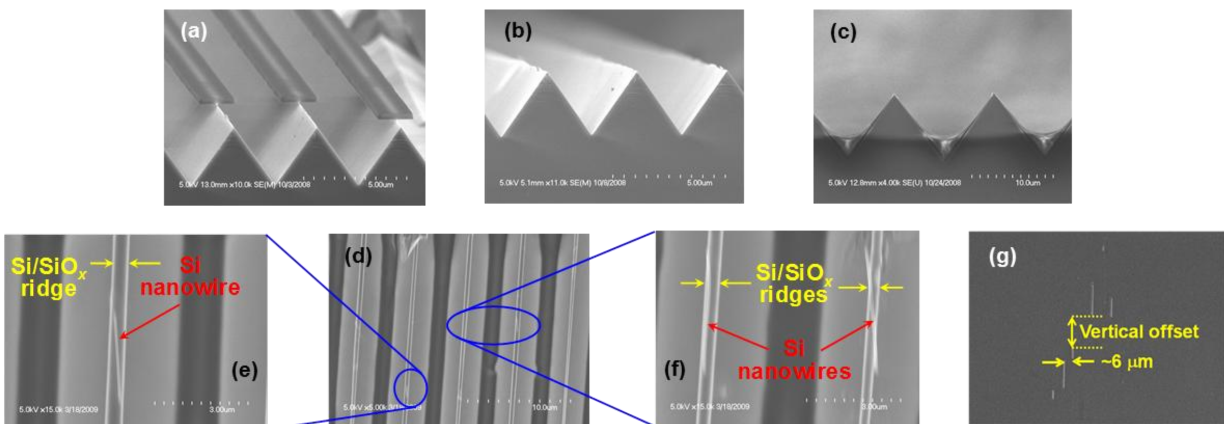

Figure 7. (a)-(f) Scanning electron micrographs (SEM) of various modular processes.[26] LER-free Si ridge arrays (a) before and (b) after the SiO_2 ribbons removal. (c) Periodic PMMA trough/Si ridge arrays. (d)-(f) Successful aligned assembly of Si nanowires onto the Si/SiO_x ridge array via electrostatics-driven selective conjugation. (g) Optical micrograph of an aligned Si nanowire array transferred onto a PDMS substrate surface.

VLS-grown Si nanowires, wrapped with native oxide, with diameter of ~100 nm were employed in our assembly experiment. Their selective attachment onto the Si ridge surface rather than the PMMA surface was accomplished through proper surface treatments. The Si nanowire surface was amine-terminated via 3-aminopropyltriethoxysilane (APTES) molecules in ethanol to become positively charged. The PMMA trough/Si ridge array surface was exposed to oxygen plasma such that the now Si/SiO_x ridge surface would be hydroxyl-terminated and negatively charged. The nanowire solution was then brought into contact with the ridge surface for the electrostatics-driven selective conjugation to occur as required in Fig. 6(d). Next the inter-ridge PMMA was removed without interfering with the assembled nanowire array as required in Fig. 6(e). Although any nonselective conjugation between the PMMA and nanowire surfaces would have been suppressed owing to the minimal coverage of APTES on the PMMA surface, this PMMA removal process effectively lifted off any nanowires that might have randomly adhered onto the PMMA surface.

Shown in Figs. 7(d)-(f) are micrographs from one of the successful attempts at aligned assembly of Si nanowires onto a periodic Si/SiO_x ridge array. Si nanowires were assembled at multiple ridge locations but not down the troughs, demonstrating the feasibility of our heterogeneous integration strategy. Finally, the periodic ridge array substrate was used as a stamping mold to transfer the assembled Si nanowires onto the receiving polydimethylsiloxane (PDMS) surface upon contact as shown in Fig. 7(g).

Although the proposed strategy has been validated, there remain several areas for future optimization. First, the nanowires within an aligned array are vertically offset as marked in Fig. 7(g). This issue can possibly be addressed by carefully designing the stamping mold. Second, the nanowires have a large variation in length. This can be rectified in

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part by improving the source nanowire length uniformity as well as perfecting the transfer yield. Third, the nanowire density within an array is rather low, which can be increased by either concentrating the nanowire solution or dispensing the solution a few more times.

3.3 VLSI-ready patterning and stamping transfer

Our second strategy for heterogeneous integration is based on lithographic patterning, etching, and stamping transfer of epitaxial nanostructures. While stamping transfer has been well developed,[9,41-45] our goal is its implementation using VLSI foundry equipment and processes to achieve multi-site concurrent formation as well as scalability to large wafer-scale. For nanofabric driver applications, epitaxial semiconductor nanowires with proper doping concentration would be required for xnwFET JL channel operation. To examine the initial feasibility of our VLSI-ready strategy, we have performed in-house Si and III-V compound semiconductor nanowire array formation and their aligned stamping transfers.

For Si nanowire array synthesis, we employed silicon-on-insulator (SOI) substrates to provide the source material whose doping level could be determined by that of the donor wafer prior to bonding. We first synthesized nanowire arrays with width ranging between 100-200 nm using standard electron-beam lithography and anisotropic dry etching. We then undercut the buried oxide (BOX) underneath the patterned Si nanowires to facilitate nanowire release during pick-up. After that, we brought the SOI substrate with patterned Si nanowires into contact with a transparent elastomeric PDMS stamp using a commercial contact aligner (Fig. 8(left)). As shown in Fig. 8(a), nanowire arrays at multiple locations were concurrently picked-up by the stamp with reasonably high yield. To prepare for the aligned stamping transfer, we have also created a simple stage setup to mount both the hosting substrate and nanowire stamp (Fig. 8(left)). Using that we have been able to release the nanowire arrays from the stamp and aligned transfer them onto the hosting silicon oxide surface (Fig. 8(b)). Moreover, we could continue to perform contact lithography with pads aligned to both ends of the nanowire array (Fig. 8(b)) demonstrating the viability of subsequent BEOL metallization.

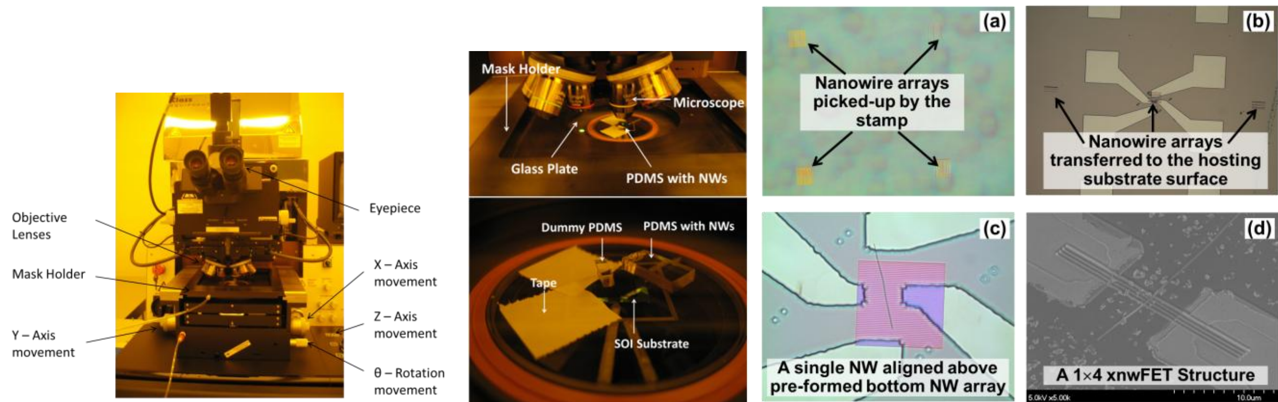

Figure 8. (left) The commercial mask aligner and developed stage setup. (a) Nanowire arrays picked-up by the stamp, and (b) transferred onto an oxide hosting substrate surface. (c)-(d) xnwFET structures synthesized by the aligned transfer of a single nanowire over a pre-formed bottom nanowire array above the hosting substrate surface.

In addition, we have attempted to construct the xnwFET (Fig. 1(a)) structure without FEM as a proof-of-concept. First, we have created a Si nanowire array above the hosting substrate (or SOI in this case) without undercutting the BOX layer. We have then followed the aforementioned procedure to pick-up, align, and transfer a single nanowire over the pre-formed nanowire array. After applying proper amount of contact pressure and time, we have also been able to demonstrate both $1\times n$ and 1×4 xnwFET structures (Figs. 8(c) and (d)) using entirely standard foundry facilities.

Moreover, we have also investigated the heterogeneous integration of high-mobility epitaxial GaAs nanowires. First, we synthesized a lattice-matched GaAs (active)/AlGaAs (sacrificial) bi-layer with *in situ* doping above a GaAs substrate using molecular beam epitaxy (MBE). The functions of the GaAs and AlGaAs layers are respectively analogous to the SOI and BOX layers in the SOI substrate discussed above. We then defined the nanowire arrays in the GaAs top layer via lithography and etching, and subsequently etched the underlying sacrificial AlGaAs layer in a self-aligned, highly selective, and isotropic manner. After that, we again brought the patterned GaAs nanowire arrays into contact with a PDMS stamp using a contact aligner to pick up the GaAs nanowire arrays. Next, we immediately transferred the arrays

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onto a hosting SiO_2-coated Si substrate, that mimicked the BEOL dielectric surface, using also the contact aligner. Confirmed in Fig. 9(a) is the successful concurrent stamping transfer of GaAs nanowire arrays with high yield, over large area, and at multiple locations. It is noted that the thermal budget to synthesize the nanowire arrays would never be seen by the hosting substrate with this strategy.

Furthermore, we have also hypothesized the device-level heterogeneous co-integration of GaAs and Si nanowires onto the same substrate surface utilizing only VLSI foundry infrastructure. First, we defined the Si nanowire arrays on an SOI substrate via lithography and etching, yet without undercutting the BOX layer. We then repeated the above GaAs nanowire array synthesis and pick-up procedures, and then stamping transferred the arrays onto the open areas of the hosting SOI substrate without pre-defined Si nanowire arrays. Shown in Fig. 9(b) are optical micrographs of co-integrated Si and GaAs nanowire arrays over large area and at multiple sites. The close proximity and thus fine granularity heterogeneous integration demonstrated here would not be possible without harnessing the alignment capability of the lithography equipment.

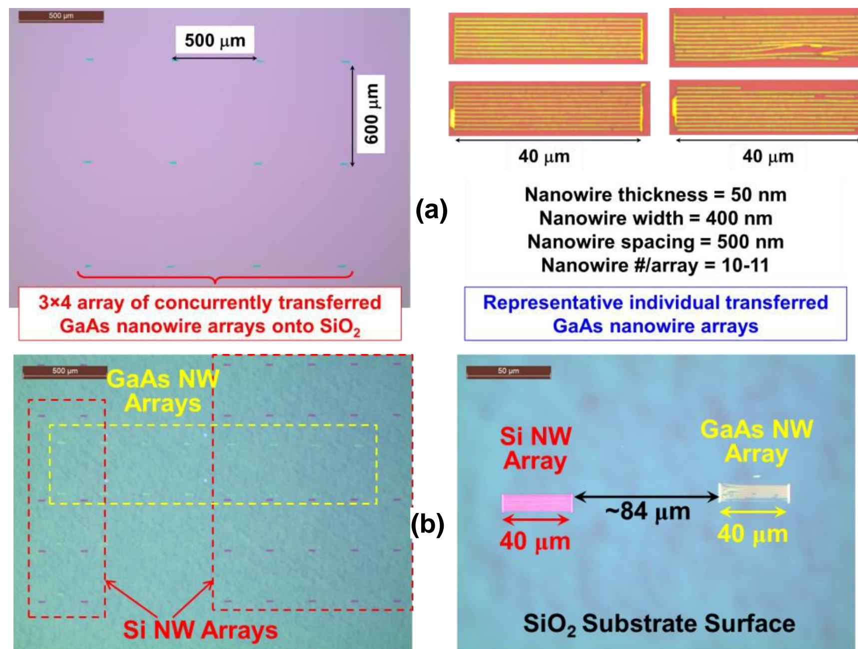

Figure 9. (a) Successful concurrent multi-site stamping transfer of GaAs nanowire arrays onto a SiO_2 substrate surface. The left optical micrograph shows a low-zoomed 3×4 array of GaAs nanowire arrays and the right image contains high-zoomed images of selected individual GaAs nanowire arrays. (b) Successful heterogeneous co-integration of GaAs and Si nanowire arrays with fine granularity. The left is a low-zoomed optical micrograph showing co-integration over large area and the right is a high-zoomed image depicting the proximity between heterogeneous technologies.

It should be emphasized that modern VLSI foundry tools and processes can indeed pattern much narrower nanowires (as compared to the current demo) using even optical or immersion lithography.[1] Many other advanced patterning techniques using co-polymer or DNA templates, or imprint lithography might also be considered to form these highly regular and periodic features. Therefore, the scalability of the initial nanowire array formation step should not be a practical concern. In addition, foundry lithography tools should also allow much better overlay accuracy to achieve much closer integration proximity and finer granularity. Ultimately, we also envision a genuine epitaxial nanostructure heterogeneous integration route using a lithography stepper and in a 'step-and-stamp' fashion.

4. CONCLUSIONS

In this paper, we review the recent developments of heterogeneous integration of epitaxial nanostructures. We have first identified the real demand for heterogeneous integration in nanoelectronics and offered our vision to introduce device-level heterogeneity in the form of computing nanofabrics. We have also reviewed the state-of-the-art fabric synthesizing

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techniques. We have then presented the novel application drivers at both the circuit-level known as Nanoscale Application Specific Integrated Circuits and at the device-level called cross-nanowire field-effect transistors. We have also outlined the heterogeneous integration technology requirements and presented two strategies – scalable and controllable *ex situ* aligned assembly, and VLSI-ready patterning and stamping transfer. Finally, we have revealed the successful concurrent heterogeneous co-integration of Si and III-V compound semiconductor epitaxial nanostructures onto the same hosting substrate over a large area, at multiple locations, with close proximity, fine granularity and high yield.

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