Spin Wave Functions Nanofabric Update

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***Abstract*— We provide a comprehensive progress update on the magnonic spin wave functions nanofabric. Spin wave propagation does not involve any physical movement of charge particles. Information is encoded in the phase of the wave and computation is based on the principle of superposition. This provides a fundamental advantage over conventional charge based electronics and opens new horizons for novel nano-scale architectures. The coupling mechanism between the spin and charge domain is enabled by the Magneto-Electric (ME) cells. Based on our experimental work we show that, an electric field of ~1MV/m would be required to obtain 90 degree magnetization rotation. The paper also provides a methodology for estimating ME cell switching energy. In particular, we show that this energy can be as low as 10aJ. In addition, we discuss different topology options and circuit styles for 1-bit/2-bit magnonic adders. Our estimates on benefits vs. 45nm CMOS implementation show that, for a 1-bit adder, ~40X reduction in area and ~60X reduction in power is possible with the spin wave based implementation. For the 2-bit adder, results show that ~33x area reduction and ~40X reductions in power may be possible.**

Keywords- Spin Wave Functions (SPWFs); magnetostriction; threshold logic; parallel counters; magnonic logic.

I. INTRODUCTION

As CMOS technology scaling reaches its fundamental limits, several new devices, state variables, manufacturing approaches, circuit styles and architectures have been explored [1-5]. Use of electron spin for computation has been identified as a promising alternative for building future nanoscale systems [6][7]. The fabric concept of Spin Wave Functions (SPWFs) nanofabrics, wherein a logic function is implemented in a single step, was introduced in [8]. This paper provides a detailed progress update on SPWFs and underlying technology.

Spin waves, also called as magnons are the collective oscillation of electrons spins in a spin lattice around the direction of magnetization [9][10]. Information may be encoded in the phase of the propagating waves and computation is based on the principle of wave superposition. It should be noted that, since spin wave propagation does not involve physical movement of charge particles, it is expected that this computational paradigm is extremely energy efficient. Spin waves coherence length can be greater than tens of micro meters (at room temperature), which makes them highly suitable for logic realization [11].

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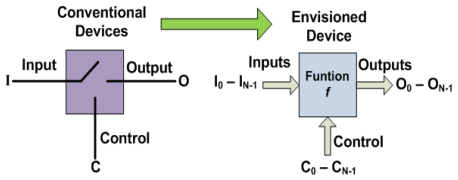

Figure 1. Devices for nanofabrics: (left) conventional switch; (right) envisioned device with alternate state variables.

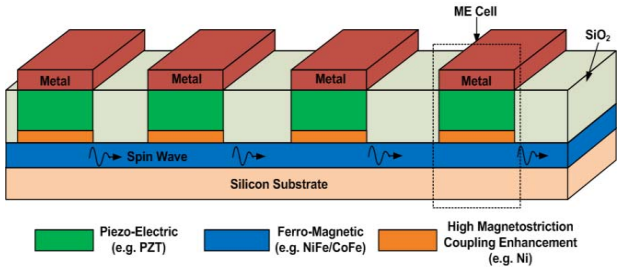

Figure 2. Physical structure of the spin wave nano-fabric showing mainly the ME cells and the spin wave bus.

The spin wave functions fabric is based on electron-spin as the state variable. Non-equilibrium physical phenomenon based devices can be made more functional than simple switches. Fig. 1 shows the basic idea of the device in conventional computational systems and our envisioned SPWF approach [8]. In the nanoscale regime, it is also essential to adopt an integrated fabric-circuit development approach. We show how the capabilities at the physical fabric level can influence circuit design aspects, and vice-versa.

Fig. 2 shows the physical fabric structure and key physical components of the spin wave based nanofabrics. It mainly consists of the ME cells and the Spin Wave Bus (SWB) [10]. While, the spin waves propagate in the SWBs with no electric current flow, the ME cells provide the mechanism for electric field control of spin waves and also realize non-volatile memory. This provides several significant advantages that include: (i) non-volatile operation which eliminates the need for separate latching circuits with significant reductions in static power dissipation; (ii) use of a Magneto-Electric element (ME) cell with electric field control of spin waves using novel materials (e.g. multiferroics) can be scaled down to the order of 40kT, minimizing dynamic power; (iii) wave superposition principle naturally enables efficient realization of threshold functions with significant reduction is logic complexity and

overall gate count; (iv) integrated fabric-circuit exploration approach enables efficient waveguide topologies and also paves way for more relaxed constraints on waveguide patterning; (v) Preserves compatibility with CMOS with respect to fabrication and electronic-magnetic-electronic interface allowing for hybrid architectures.

The main contributions of this paper include: i)An update on the experimental work on voltage controlled magnetization rotation for ME cells; ii) A methodology for estimating the ME cell switching energy; iii) Initial analysis on possible ways of reducing the ME cell switching energy; iv) A vision for break-through nano-scale fabric development with integrated fabric-circuit explorations; v) Different circuit styles, ME cell capabilities explored with 1-bit/2-bit adders as examples vi) Projected comparisons vs. 45nm CMOS custom designs.

The rest of the paper is organized as follows. Section II presents the updates on voltage controlled magnetization rotation in ME cells along with energy estimates. Section III presents the basic methodology for magnonic logic design. We present our initial progress towards integrated fabric-circuit explorations in Section IV. This section also shows different topology options and circuit styles that can be used for magnonic logic design. Section V presents a discussion on projected benefits vs. 45nm custom CMOS adder designs. Section VI concludes the paper.

II. Physical Fabric For Magnonic Logic

Fig. 2 shows the physical fabric structure and key physical components of the spin wave based nanofabrics. It mainly consists of the ME cells and the Spin Wave Bus (SWB). Eq. 1 shows the Landau-Lifshitz-Gilbert (LLG) formulation that is widely used for spin wave transport modeling [12][13].

$$\frac{\partial \vec{m}}{\partial t} = -\gamma\left[\vec{m} + \vec{H}_{eff}\right] + \alpha\left[\vec{m} * \frac{\partial \vec{m}}{\partial t}\right] \quad (1)$$

Where $\vec{m} = \vec{M}/_{M_s}$ is the unit magnetization vector, M_s is the saturation magnetization, γ is the gyro-magnetic ratio and α is the phenomenological Gilbert coefficient. Prior research has shown that this formulation has good agreement with experimental data [11] on spin wave transport (e.g. in NiFe thin films).

The ME cells provide the essential coupling mechanism between the spin and charge domain. Based on the voltage polarity of the primary inputs, spin waves with corresponding phase are excited. In addition to providing the I/O mechanism, the ME cells also enable non-volatile storage of information via electric field control. In magnonic logic circuits, the ME cells are also used to provide amplification of intermediate waves to realize useful logic functionality (example shown in section IV). ME cells may also be used on the interconnect SWBs for signal restoration of propagating spin waves. Since, ME cell performs several important functions in the spin wave fabric, the primary objective of our theoretical and experimental work is to study the ME cell switching characteristics and energy consumption. In this section, we report the progress on ME cell characterization and also discuss potential techniques to further optimize ME cell switching characteristics.

A. Experimental Data on Voltage Controllel Magnetization Rotation

A critical requirement for energy efficient generation, modulation, and detection of spin waves is the control of magnetization using electric fields (i.e. voltage) as opposed to currents (e.g. spin transfer torque or inductive coupling to current loops [14-16]). To realize voltage control of magnetization, layered heterostructures of piezoelectric and ferromagnetic films can be used [17]. A critical requirement for this scheme is that the magnetic films need to have a large magnetostriction coefficient, while still maintaining other properties critical to spin wave propagation such as low damping factor and small coercive field [14-16]. The saturation magnetization (M_s) of the magnetic field needs to be optimized based on tradeoffs between Magneto-Electric coupling and spin wave propagation frequency. While we can expect higher Magneto-Electric coupling with small M_s, a large M_s is desirable since it increases the spin wave propagation frequency range (hence bandwidth). A possible optimization approach could involve using bilayers, where a soft, low-loss, high-M_s spin wave bus material (e.g. NiFe or CoFeB) is

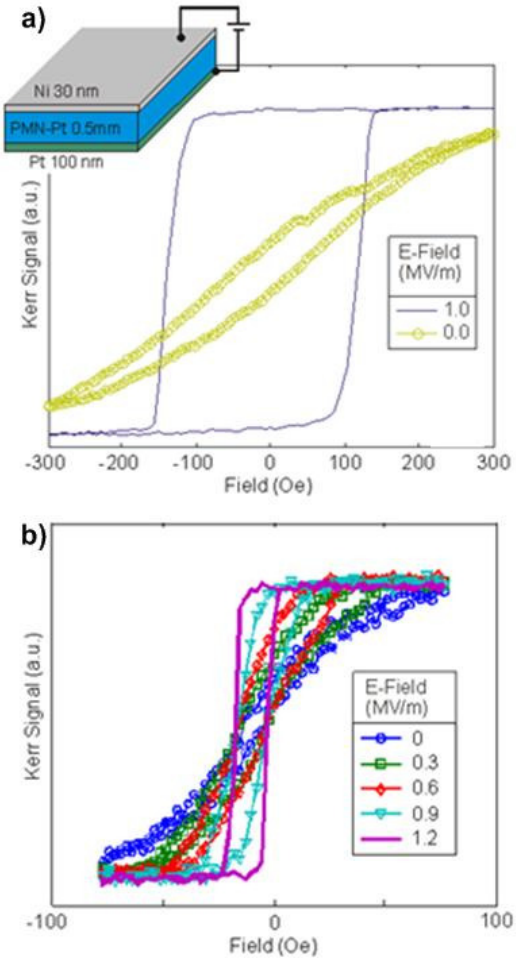

Figure 3. Magnetization rotation by electric field in (a) 30 nm Ni films and (b) 30 nm Ni – 30 nm CoFeB bilayers on a piezoelectric PMN-PT substrate. A full 90 degree reorientation of the magnetic easy axis is achieved with fields ~1MV/m.

exchange-coupled to a low-M_s, high-magnetostriction coupling enhancement layer (e.g. Ni or Co).

Fig. 3 shows an example of Magneto-Electric voltage control of magnetization for ferromagnetic single and bilayers. Fig. 3a shows Magneto-Optical Kerr Effect (MOKE) measurements on a 30 nm Ni film deposited on a piezoelectric PMN-PT substrate. A 90 degree reorientation of the easy axis can be observed with fields ~1 MV/m. Note, however, that the Ni film exhibits a rather large coercivity (~100 Oe), which is undesirable for high-frequency spin wave propagation. Fig. 3b illustrates a similar effect where a 30 nm CoFeB film is added to the structure. While the magnetization rotation is achieved with a similar field, the coercivity is reduced to ~10 Oe, significantly improving the soft magnetic characteristics required for the spin wave bus material.

B. ME Cell Switching Energy Estimates

In section II.A, experimental data on voltage-controlled magnetization rotation in the synthetic multi-ferroic (piezoelectric/magnetostrictive) structure was presented. Here, we provide more rigorous estimates on the energy consumed by ME cells and in general for spin wave circuits. We would like to reiterate that, spin wave propagation does not involve physical movement of charge and thereby, there is no power consumption associated with wave propagation in the SWB. However, external energy is needed to excite input spin wave signals and to assist the output ME cell switching. In both cases, an electric energy is used to alter magnetization via Magneto-Electric coupling in the ME cells. The total energy E is defined by the number of the ME cells per circuit N_{ME} and the energy required for magnetization rotation in one cell E_{ME}:

$$E = N_{ME} \times E_{ME}.$$

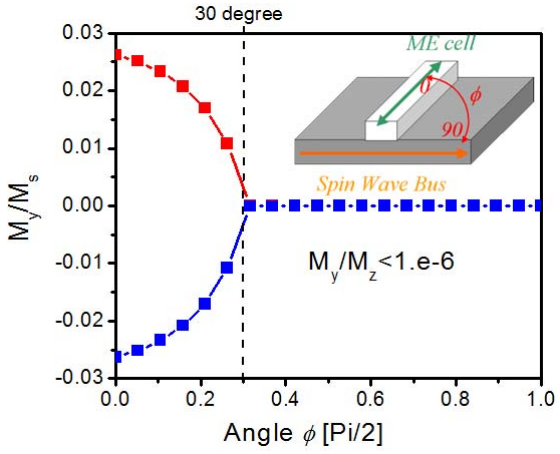

Figure 4. Results of numerical simulations illustrating the magnetization states (±My) of the ME cell as a result of the interplay between the shape anisotropy field of the ME cell and exchange coupling with the spin wave bus. ME cell switching by spin wave is possible at easy axis rotation by 30 degree.

The ME cell structure represents a parallel plate capacitor consisting of a non-magnetic metallic layer (e.g. Al), a layer of piezoelectric material (e.g. PZT), and a conducting magnetostrictive material (e.g. Ni). As a conservative estimate, the total energy consumed by ME cell per switch can be calculated as follows:

$$E_{ME} = \frac{CV^2}{2} = \frac{\varepsilon_0 \varepsilon_r A}{2d} V_{\pi/2}^2 \quad (2)$$

where ε_0 is the vacuum permittivity, ε_r is the relative permittivity of the piezoelectric, A is the surface area of the ME cell, d is the thickness of the dielectric layer, $V_{\pi/2}$ is the voltage required for 90 degree magnetization rotation. In order to provide high-frequency spin wave excitation, the thickness of the piezoelectric layer should be adjusted to the spin wave frequency (e.g. d=0.8um for resonance frequency of 1GHz). Taking the following data: ε_0=8.854×10^{-12} F/m, ε_r = 1700 for PZT, A=100nm×100nm, d=0.8um, $V_{\pi/2}$=1MV/m×0.8um=0.8V, we would require ~60aJ of energy per ME cell.

The energy per switch scales proportional to the size of the ME cell and can be reduced by optimizing the material structure and switching dynamics. It is also possible to reduce the switching energy by decreasing the applied voltage (e.g. accomplish switching with less than 90 degree easy-axis rotation). ME cell is magnetically coupled with spin wave bus within the circuit. It may be possible to exploit the interplay between the magnetic field of the ME cell (e.g. shape anisotropy) and the magnetic field of the spin wave bus (exchange coupling) to reduce the switching angle.

Fig. 4 shows the results of micromagnetic modeling illustrating the position of the two magnetization states of the ME cell as a function of the angle between the in-plane and cross-plane magnetic fields. The simulations are done in the strong coupling limit (the in-plane magnetic field produced due to the exchange coupling to the spin wave bus is much stronger than the cross-plane anisotropy field of the ME cell). In this case, the ME switching is possible with magnetization rotation about only 30 degree. The later translates in the possibility to reduce the switching electric field from 1MV/m to about 0.4M/m, $V_{\pi/6}$=0.4MV/m×0.8um=0.32V, resulting in the energy per ME cell as low as ~10aJ.

In general, the minimum energy per switch is limited by the energy barrier between the two magnetization states of the ME cell. To be practical, the energy barrier should be about 40kT, where k is the Boltzmann constant, and T is the ambient temperature. The obtained experimental data shows a possible pathway towards achieving ultra-low power consuming logic devices with orders of magnitude advantage over scaled CMOS. It should be noted that the obtained data on voltage-controlled magnetization rotation were obtained at DC measurements and require further validation at high-frequency switching regimes.

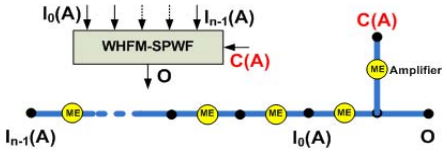

Figure 5. Weighted High Fan-in Majority Function Device (WHFM). (top left) Block diagram (bottom) Schematic representation with linear waveguide and ME cells for input amplification [8].

III. Magnonic Logic Design and Spin Wave Functions

Magnonic circuits exploiting wave interference enable accomplishing complex logic functions such as high fan-in majority function(s) in a single computational step. Fig. 5 shows an example SPWFs (***Spin Wave Logic Functions***), one of the general circuit styles proposed, realizing majority functions with weighted inputs. The concept of SPWFs was first introduced in [8], and these elementary functions were identified as key building blocks for magnonic logic design.

The wave interference phenomenon in the spin wave fabric naturally enables efficient realization of threshold or majority logic functions. Threshold gates fundamentally realize more complex logic functions compared to conventional Boolean gates (AND, OR etc.); consequently, reducing the number of logic levels and the overall gate count required to realize a given circuit [18-20]. However, since the physical implementations (e.g. CMOS based) of the threshold gates are known to be highly complex, this logic style has had little impact on CMOS VLSI design.

TABLE I. 2-bit Adder Comparison vs. 45nm NCSU PDK Based Custom CMOS Layout

Full Adder-inputs				Full Adder-outputs	
A	B	C_{in}	# of 1's in (A,B,C_{in})	C_{out}	Sum
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	2	1	0
1	0	0	1	0	1
1	0	1	2	1	0
1	1	0	2	1	0
1	1	1	3	1	1
(3;2) counter					

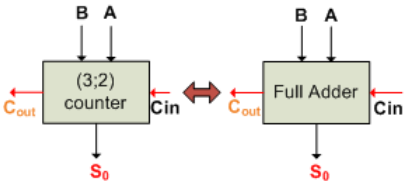

Figure 6: (3;2) counter with three inputs and two outputs equivalent to a 1-bit full adder.

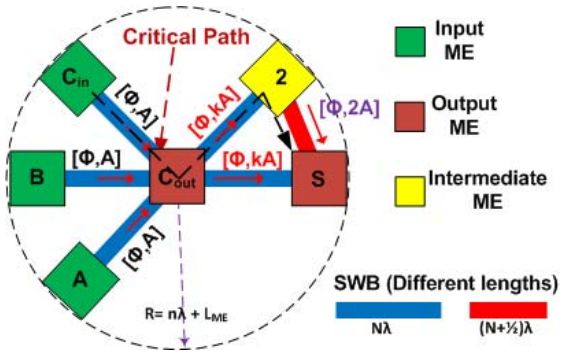

Figure 7: Weighted majority SPWF based 1-bit full adder layout.

On the contrary, the SPWF approach leverages on the wave interference phenomenon and thus no special gate/component is required to realize the majority function. Moreover, significant reduction is power consumption is also expected given the fact that spin wave propagation does not involve any charge propagation. In this work, we illustrate this principle based on our evaluations on adder designs implemented using parallel counters.

A. Full Adder Design Using (3;2) Parallel Counters

Parallel counters are known to be highly efficient for implementing high-speed arithmetic circuits [21]. Parallel counters are digital circuits with 'n' inputs and $\log_2(n+1)$ output bits representing the number of 1's in the 'n' input bits set [21]. Realization of parallel counters based on the principle of threshold logic, enables highly optimal circuits; with the implementation style being suitable for wave interference phenomenon. Table 1 shows the truth table for a (3;2) counter. It can be observed that, a (3;2) counter realizes the same functionality as 1-bit full adder (as shown in Fig. 6) and thus a (3;2) parallel counter is identified as a basic building block for realizing large adder designs. Fig. 7 shows the weighted SPWF based implementation that uses only 6 ME cells. This shows that significant complexity reduction can be expected with the SPWF based implementation.

IV. Integrated Fabric and Circuit Exploration

Historically, the first step in a new computational paradigm is the development of efficient devices. Circuit designers and architects then use these devices to build bigger systems. We argue that for development of breakthrough post-CMOS nanofabrics, an integrated fabric-circuit exploration is necessary. Our efforts towards developing new architectures using magnonic logic places strong emphasis on cross-cutting issues and integrated exploration across multiple design levels aimed at solving problems from a particular fabric perspective.

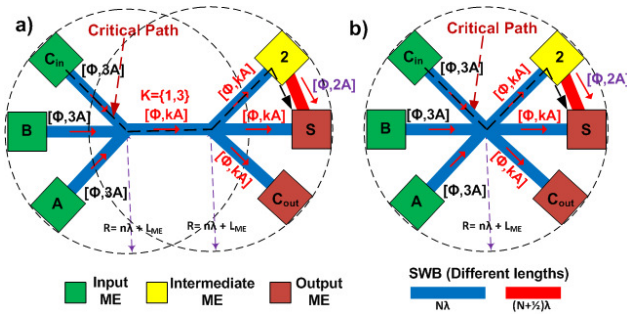

Figure 8: a) Intermediate design showing circuit topology changes that enable realization of 1-bit adder without Amplitude Tracing MEs. b) Final 1-bit adder without Amplitude Tracing MEs (more compact).

Two type of ME cells are discussed; one with *Amplitude Tracing* capabilities and other without *Amplitude Tracing* capabilities. Dual-rail logic based inversion-free designs are presented in section IV.B showing how circuit styles can impact the manufacturing and physical fabric related constraints.

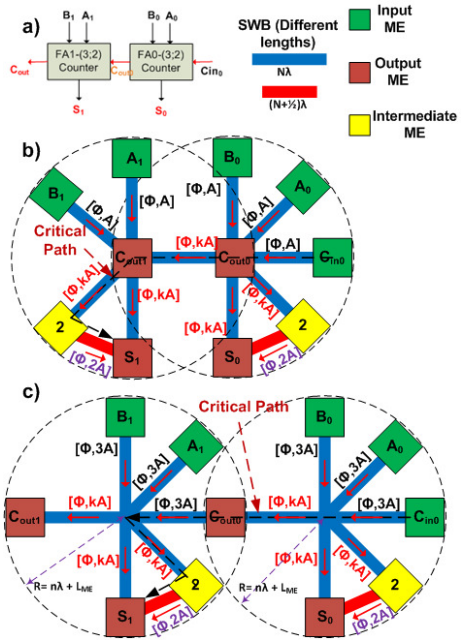

Figure 9: a) Block diagram of 2-bit ripple adder. b) SPWF implementation of 2-bit adder with Amplitude Tracing MEs. c) SPWF implementation of 2-bit adder without Amplitude Tracing MEs.

A. Adder Desings With and Without Ampltiude Tracing MEs

Amplitude Tracing refers to the ability of the ME cells to re-generate new spin waves with variable/dynamic amplitudes depending on the amplitude of the incoming spin waves. One of the primary constraints for the design shown in Fig. 7 is that it requires re-generation of spin waves with variable/dynamic amplitudes. For example, in Fig. 7 amplitude of the wave from the C_{out} ME cell to the *Intermediate* ME and the *SUM* ME will be dynamic based on the interference of the three inputs waves. This may require additional feedback mechanism in the ME cells to trace both phase and amplitude of incoming waves. The ME cell structure discussed in section II, is phase-only ME cell

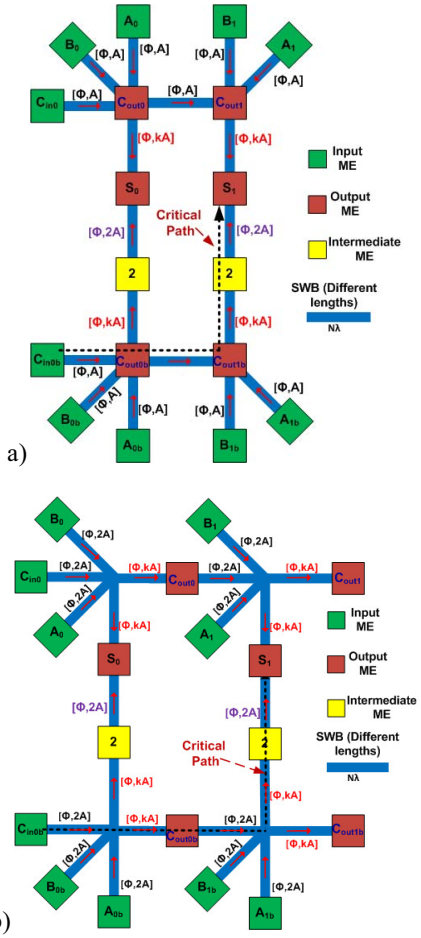

Figure 10: a) Inversion free 2-bit adder design with Amplitude Tracing MEs. b) Inversion free 2-bit adder design without Amplitude Tracing MEs.

without any amplitude tracing capabilities. In contrast, the design in Fig. 8 does not have this requirement of ***Amplitude Tracing***. Here the waves after interference (with additional information encoded in the amplitude of the resultant wave) are preserved for further computation. Thereby, all ME cells generate waves of ***fixed*** amplitude. This can significantly reduce the complexity of ME cells.

Fig. 9 shows the realization of 2-bit ripple adder using 2 (3;2) parallel counters. Both designs, with and without Amplitude Tracing MEs are shown. Note that the second design (Fig. 9.c) uses the same number of ME cells as the first design (Fig. 9.b). However there is only a slight penalty in area for the second design which is acceptable given the fact that it significantly relaxes the constraints on ME cell design. Another benefit of the second design is that it reduces the number of ME cells on the critical path (as shown in Fig. 9). A detailed comparison of the adder designs and projected benefits vs. CMOS is presented in section V.

B. Inversion-Free Full Adder Design

The designs shown in Fig. 7-9, require realization of odd phase shifts for the wave propagating from the intermediate MEs to the SUM ME cells. This may enforce more stringent

waveguide patterning requirements to achieve accurate phase shifts, and may also affect the spin wave propagation velocity.

Fig. 10 shows a SPWF 2-bit adder layout based on dual-rail principle that eliminates the need to have any intermediate inversion in the design. Thereby, relative to the designs shown in Fig. 7-9, this design has more relaxed patterning constraints. A key observation here is that, in a ripple adder circuit only the carry signals are propagated across different bits, thus duals of only the 'carry-out' signals are need; thereby reducing the area and power consumption overhead. In addition, as in the case of the design without Amplitude Tracing MEs (Fig. 8, Fig. 9c), in Fig. 10.b, the number of ME cells on the critical path in this design is reduced leading to relatively less delay.

V. PROJECTTED BENEFITS VS. CMOS

In this section, we present our initial evaluations of the proposed adder designs vs. equivalent 45nm CMOS design. The assumptions used for these evaluations are also presented along with the evaluation methodology. Table II and Table III show the power, delay and complexity comparisons for both the 1-bit and 2-bit adders. Projected benefits vs. CMOS are shown for all design styles; Amplitude Tracing (AT), W/O Amplitude Tracing (W/O AT) and the Inversion Free (IF) designs. Table II and Table III also show how the SPWF designs would compare with the corresponding CMOS designs without the presence of I/O ME cells. This type of evaluation would enable us to estimate the benefits of SPWFs whose inputs are not the direct primary inputs. In this case, we assume that the inputs are directly available as input spin waves without any I/O ME cells.

A. Fabric Parameters

In section II, the experimental data related to the ME cell switching was presented. For SPWF design evaluation, ME cell dimension of 100nm*100nm with a switching delay of 100ps is used. For power estimation, ME cell switching power is assumed to be 100nW/operation, based on the ME cell switching energy estimates discussed in section II.B. For the Spin Wave Bus (SWB), a wave propagation delay of 10^4m/s is assumed [10]. All the CMOS design (Fig. 11) evaluations were done on a custom 45nm CMOS design (using NCSU 45nm PDK)based on Hspice simulations.

B. Evaluation Methodology

The delay calculation for both the SPWF and the CMOS designs is determined by the amount of logic and interconnect along the critical path. For a 2-bit adder, the critical path is from the C_{in0} to S_1. SPWF design delay is determined by the number of ME cells and length on the SWB encountered along the critical path. For example, for the design shown in Fig. 9.c, there are 4 ME cells along and the delay is ~535ps including the delay on the SWB. The worst case transition delay for the CMOS design is determined using Hspice simulations on the spice netlist extracted from the layout shown in Fig. 11.

Power consumption for the SPWF designs in mainly associated with the ME cell switching. The overall power consumption is estimated based on the number of ME cells in the design. The power consumption for the 45nm CMOS layout is calculated based on Hspice simulations. The average power over 40 trails with 1000 random transitions in each is reported here. Area for both the SPWF and CMOS designs are calculated directly from the layouts of the adder designs.

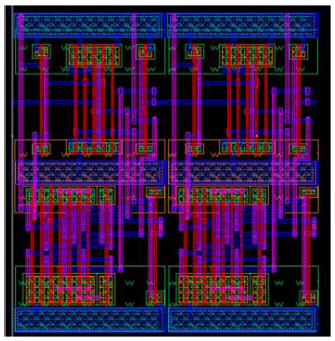

Figure 11: NCSU 45nm PDK based 2-bit CMOS adder layout.

C. Discussion on Projected Benefits vs. CMOS

Table II and Table III show the overall comparison results. As expected, these results show that SPWF designs are highly power efficient. Table II shows an estimated power reduction of 60X for the 1-bit regular SPWF w/o AT adder design. For the 2-bit SPWF version, a reduction of up to 40X is expected. This huge reduction in power consumption is also attributed to the significant reduction in overall design complexity of the SPWF designs. The CMOS design requires up to 64 transistors for the 2-bit adder, while the SPWF design needs only 11 ME cells for the regular Amplitude Tracing Free designs (Fig. 9.c). These results on estimated power reduction show that the magnonic logic direction is one of the promising options for post-CMOS chip designs.

TABLE II. 1-BIT ADDER COMPARISON VS. 45NM NCSU PDK BASED CUSTOM CMOS LAYOUT

Fabric	Design	Delay	Power	Complexity
CMOS	Custom	~250ps	~36.5µW	Area ~= $20\mu m^2$ Transistor Count = 32
SPWF with I/O ME	With AT	~475ps	~0.6µW	Area ~= $\pi * (4\lambda)^2$= $0.5\mu m^2$ ME Count = 6
	W/O AT	~375ps		
SPWF without I/O ME	With AT	~275ps	~0.2µW	Area ~= $\pi * (3\lambda)^2$= $0.28\mu m^2$ ME Count = 2
	W/O AT	~175ps	~0.1µW	Area ~= $\pi * (3\lambda)^2$= $0.28\mu m^2$ ME Count = 1

[AT = Amplitude Tracing, IF = Inversion Free, λ=100nm, ME cell = λ*λ, ME delay = 100ps, Wave velocity = 10^4 m/s, ME switching power =100nW]

Table II and Table III show that the overall delays of the SPWF and CMOS design are comparable. While the results presented in [8], show a large performance benefit for high fan-in logic functions (with inherent parallelism in the operations), these results show that small designs with bit-wise dependencies may not benefit in terms of performance with the SPWF implementations without further improvement on ME cell delay.

Another significant benefit observed for the SPWF designs is the reduction in the overall area. For regular w/o AT designs,

TABLE III. 2-BIT ADDER COMPARISON VS. 45NM NCSU PDK BASED CUSTOM CMOS LAYOUT

Fabric	Design	Delay	Power	Complexity
CMOS	Custom	~400ps	~44.5µW	Area ~= 40µm^2 Transistor Count = 64
SPWF with I/O ME	With AT	~605ps	~1.1µW	Area ~= 12λ*8λ= 0.96µm^2 ME Count = 11
	W/O AT	~535ps		Area ~= 15λ*8λ= 1.20µm^2 ME Count = 11
	IF-AT	~600ps	~1.8µW	Area ~= 12λ*17λ= 2.04µm^2 ME Count = 18
	IF-W/O AT	~530ps		Area ~= 15λ*17λ= 2.55µm^2 ME Count = 18
SPWF without I/O ME	With AT	~375ps	~0.4µW	Area ~= 9λ*6λ= 0.54µm^2 ME Count = 4
	W/O AT	~295ps	~0.3µW	Area ~= 11λ*6λ= 0.66µm^2 ME Count = 3
	IF-AT	~370ps	~0.6µW	Area ~= 9λ*13λ= 1.17µm^2 ME Count = 6
	IF-W/O AT	~290ps	~0.4µW	Area ~= 11λ*13λ= 1.43µm^2 ME Count = 4

[AT = Amplitude Tracing, IF = Inversion Free, λ=100nm, ME cell = λ*λ, ME delay = 100ps, Wave velocity = 10^4 m/s, ME switching power =100nW]

an area reduction of up to 40X is possible for the 1-bit adder (Table II). For the 2-bit adder a reduction of up to 33X is shown in Table III. As mentioned earlier, these benefits are mainly due two factors; one due to majority logic based implementations and other due to the highly efficient/simple majority logic realization using spin wave interference.

Our evaluation also shows that, SPWF design may even have larger benefits when all the inputs are directly available as incoming spin waves (without any I/O ME cells). We can expect up to 150X reduction in overall power consumption, up to 60X area benefit for the 2-bit regular w/o AT adder design (Table III). Similar benefits are also seen for the 1-bit adder design as shown in Table II. Due to reduction in the number of ME cells on the critical path and reduction of SPWF area, a delay reduction of up to 25% can also be expected for these internal SPWF based circuits.

VI. CONCLUSION

Magnonic logic with electron spin as the state variable is one the promising post-CMOS fabric option. Magneto-Electric cells provide the necessary I/O mechanism, amplification and also enable non-volatility; thereby the ME cell is identified as a key physical component. Experimental data based on MOKE measurements show that ~1MV/m of electric field would be required for 90 degree magnetization rotation. For this field requirement, ~60aJ of energy would be required for ME cell switching. The field requirements can be further reduced with optimizations based on ME cell dimension, material structure and the underlying switching dynamics. We show that the ME cell switching energy can be as low as 10aJ by limiting the magnetization rotation to 30 degrees (~0.4MV/m electric field). Initial explorations on integrated SPWF fabric-circuit development are also shown based on the Amplitude Tracing and without Amplitude Tracing designs. Alternate circuit styles enable realization of inversion-free designs with relaxed waveguide patterning constraints. Our estimates on benefits vs. 45nm CMOS implementation show that, for a 1-bit adder, ~40X reduction in area and ~60X reduction in power is possible with the spin wave based implementation. For the 2-bit adder, results show that ~33x area reduction and ~40X reductions in power may be possible. In future, possible approaches to reduce the overall number of ME cells along the critical path of the design and optimizations at physical level to reduce the ME cell delay will be explored.

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