Embedded Processors based on Spin Wave Functions (SPWFs)

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***Abstract*—Spin Wave Functions (SPWFs) realize computation with spin waves, offering several benefits and new features over CMOS. SPWF technology potentially opens up new directions for designing microprocessors with increased capabilities over current implementations. Towards this end, as a preliminary work an 8-bit embedded processor is explored here using SPWFs and evaluated in terms of its power, area and performance using analytical estimates. A CMOS 8-bit processor implemented in an equivalent technology node is synthesized with CAD tools for comparison. Estimates show that the SPWF processor can have up to 40x lower power and 27x smaller area, thus showing great potential for realizing game-changing microprocessors in future.**

Keywords—SPWF, spin, embedded processor, CMOS.

I. Introduction

Spin Wave Functions (SPWFs) [1][2] have been proposed for post-CMOS computing. They use magnetic spin waves for computation to overcome the fundamental bottlenecks of power and heat dissipation with CMOS. Spin waves are collective excitation of electrons in ferromagnetic guides and have been demonstrated experimentally at room temperature [1]. SPWFs offer new features and benefits [1]-[3] which potentially change conventional assumptions for processor micro-architecture, thus opening completely new avenues for designing microprocessors with increased capabilities. SPWF performance is less sensitive to high fan-in leading to more compact circuits, and it supports multi-level (more than 2 states) communication with waves which reduces wiring requirements. Due to lower complexity in computation and communication, in principle SPWF processors may be capable of a much higher degree of parallelism (more than 4-way instruction issue, a limitation of CMOS technology due to exponential increase in complexity). SPWF memory implementation is identical to logic, with grid-based waveguides and ME-cells for control. This can (i) merge computation with memory leading to a distributed architecture with a lesser degree of localization for execution and memory units, further reducing communication requirements; and (ii) potentially surmount the memory-wall problem that impacts CMOS processors, because SPWF logic and memory performance scale identically. It may lead to a completely different memory organization than what is seen today. Also, absence of charge transport for computation yields orders of magnitude power benefits vs. CMOS which considerably improves performance-per-watt metric, and non-volatility allows an *instant-on* processor realization. While much work is needed to explore all possibilities with SPWF technology, in this concept paper we explore the feasibility and benefits of SPWF-based 8-bit embedded processor vs. CMOS 8-bit AVR processor [4].

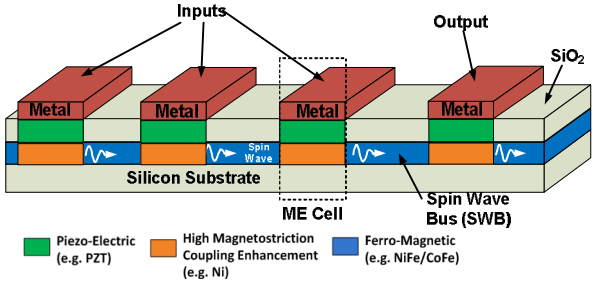


Fig. 1. Physical components in spin wave functions (SPWFs) computing fabric.

The main components of SPWFs [1] include Magneto-Electric (ME) cells and Spin Wave Bus (SWB) as shown in Fig. 1. The ME cell performs several functions such as I/O coupling, amplification, latching and synchronization. Spin waves propagate and perform computation through wave interference in the Spin Wave Bus (SWB).

II. 8-Bit SPWF Embedded Processor Architecture

The architecture for an SPWF 8-bit embedded processor is shown in Fig. 2. We envision an *instant-on* processor where the non-volatile ME cells themselves (capable of latching data) store the machine state information, without the need to write back the machine state to a separate memory unit. These non-volatile ME cells also enable a unified architecture (ALU fused

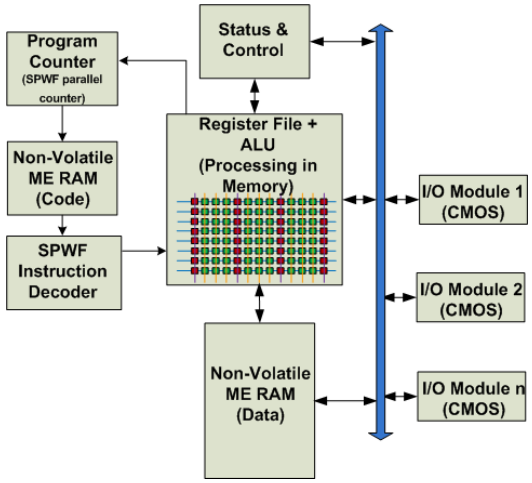
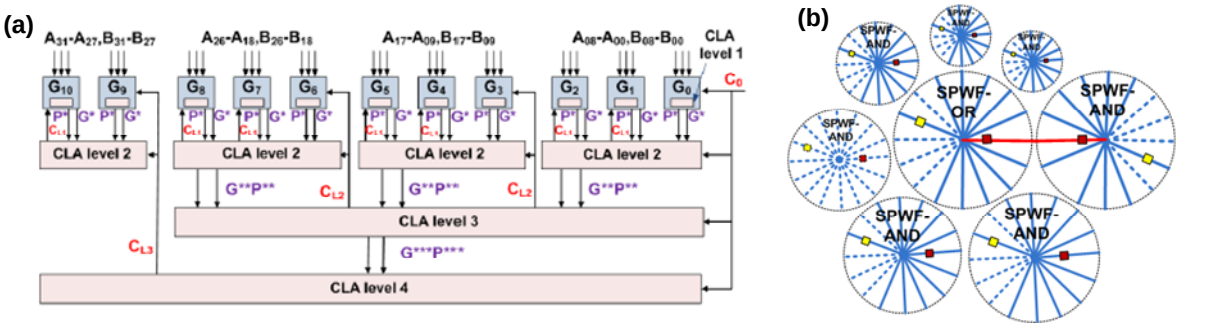


Fig. 2. SPWF 8-bit embedded processor architecture.



CMOS CLA Delay

$$Delay = \Delta g + (\log_B N - 1) * 2 * \Delta g + \log_B N * 2 * \Delta g + 2 * \Delta g$$

SPWF CLA Delay

$$Delay = 2 * \left[\frac{NP_{ME}}{2\pi} + KL_{ME}\right] * \frac{1}{V_{Spin}} + K * ME_{Delay}$$

Fig. 3. Carry look-ahead adder implemented with (a) CMOS; and (b) SPWFs [5]. In the equations for delay estimation, Δg – Gate delay based on 45nm Nangate standard cell lib.; N – Number of inputs; B – Blocking factor; L_{ME} – ME cell width; P_{ME} – ME cell pitch; ME_{Delay} – ME cell switching delay; V_{Spin} – Propagation velocity of spin waves; and K – Number of ME cells on critical path.

with register file), thus eliminating the need for a separate register-file. This leads to a significant reduction in area. In addition, the main blocks in the ALU such as carry look-ahead (CLA) adders are much more efficiently implemented with SPWFs. This is because the CLA unit can be implemented in a single stage with two-level SPWF logic [5], even at higher bit-widths. A CMOS implementation uses multiple CLA units for high bit-width adders due to fan-in limitations (see Fig. 3). These factors significantly reduce circuit complexity for SPWF arithmetic circuit implementations and, in conjunction with the fact that there is no charge transport involved, result in area and power benefits. In addition, memory blocks are non-volatile and can be supported with ME cells organized in a grid waveguide layout with readout at the end of each row. Some minimal control is necessary in the electrical domain.

III. Evaluation and Comparison with CMOS

Area calculation of SPWFs-based designs was done assuming ME cell dimensions of 2µm*2µm, based on what can be experimentally achieved currently. Feature size scaling limits are similar to CMOS since manufacturing will have to rely on lithography for wave guide creation. The comparison is therefore done with 1.5µm CMOS. Performance/clock speed is based on critical path analysis, which includes ME cell switching delay and wave propagation delay along the critical path. The ME cell is assumed to have a switching delay of 10ns. Spin wave group velocity is assumed to be 10^4m/s for calculating spin wave propagation delay [6]. Since spin wave propagation does not involve any charge transport, power consumption for SPWFs designs are mainly from ME cell switching activity. Based on numerical simulations and by using a simple capacitor approximation, ME cell switching energy is estimated to be as low as 3.85fJ per operation.

TABLE I. 8-Bit Embedded Processor Evaluation

	Processor Logic Core Comparison		
	Area	***Power***	***Performance (delay on ALU critical path)***
SPWF (2µm)	0.3 mm^2	0.25mW	~40ns
CMOS (1.5µm)	8 mm^2	10mW	~15ns

For CMOS, the area, power and delay numbers are calculated from the Verilog implementation by synthesis of a generic 8-bit processor [4] core using Design Compiler with 45nm PDK, and scaled up to the nearest 1.5µm CMOS technology node (to compare it with equivalent SPWF-based designs). The following rules are used for scaling – area is scaled by 2X for every technology node, the delay is scaled by 30% every generation and the power is scaled by (V_{DD} scaling)^2 [7]. For 45nm the V_{DD} is 0.9V and for 1.5µm the V_{DD} is 5V. The results of the comparison are shown in Table I.

IV. Conclusion

The feasibility of an 8-bit embedded processor with Spin Wave Functions (SPWFs) was explored and evaluated. Analytical estimation based on initial design shows that SPWF-based processor may have up to 40x lower power and 27x smaller area vs. CMOS. While further exploration is necessary, SPWF technology can be game-changing for implementing future microprocessors and embedded systems.

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