Spin Wave Nanofabric Update

J. G. Alzate, P. Upadhyaya, M. Lewis, J. Nath, Y. T. Lin, K. Wong, S. Cherepov, P. Khalili Amiri, K..L. Wang, Electrical Engineering Department, University of California - Los Angeles
J. Hockel, A. Bur, G. P. Carman, Mechanical and Aerospace Engineering Department, University of California – Los Angeles
S. Bender and Y. Tserkovnyak, Department of Physics and Astronomy, University of California - Los Angeles
J. Zhu, Y-J Chen, I. N. Krivorotov, Department of Physics and Astronomy, University of California - Irvine
J. Katine, Hitachi GST Research Center, San Jose
J. Langer, Singulus Technologies AG, Kahl am Main, Germany
P. Shabadi, S. Khasanvis, S. Narayanan, C. A. Moritz, Electrical and Computer Engineering Department, University of Massachusetts in Amherst, Amherst
A. Khitun, Electrical Engineering Department, University of California – Riverside, Riverside, California, USA
akhitun@engr.ucr.edu

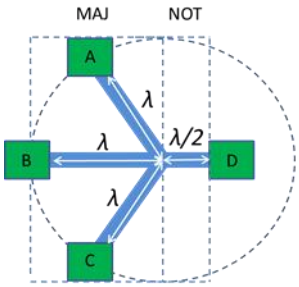
***Abstract*— We provide a progress update on the spin wave nanofabric. The nanofabric comprises magneto-electric cells and spin wave buses serving for spin wave propagation. The magneto-electric cells are used as the input/output ports for information transfer between the charge and the spin domains, while information processing inside the nanofabric is via spin waves only. Information is encoded into the phase of the propagating spin wave, which makes it possible to utilize waveguides as passive logic elements and take the advantage of using wave superposition for data processing. This provides a fundamental advantage over the conventional transistor-based logic circuitry allowing for functional throughput enhancement and power consumption minimization at the same time. We present recent accomplishments in the magneto-electric element development and integration with spin wave buses. In particular, we show the excitation and detection of the spin waves via multiferroic elements. In addition, we present different approaches to magnonic logic circuit engineering and provide the comparison with CMOS by mapping the designs to 45nm NANGATE standard cell libraries. The estimates show more than 40X power reduction and 53X area reduction for magnonic circuits. These results illustrate the potential advantages over conventional charge based electronics that could be a route to beyond CMOS logic circuitry.**

Keywords- spin wave, multiferroic, magnonic logic

I. INTRODUCTION

There is a great deal of interest to alternative state variables, novel logic devices and computational nano-architectures able to overcome the challenges associated with further CMOS scaling and provide a route to a less power consuming and more functional logic circuitry [1]. Magnonic nanofabric is one of the promising approaches aimed to benefit from using magnetization as a state variable and spin waves for information transmission and processing [2]. It offers an original way of utilizing both the amplitudes and the phases of the spin wave signals for logic functionality. The most appealing advantage of this approach is the ability to implement logic functions in a single step, so called Spin Wave Functions (SPWFs) [3]. This work presents an overall progress update including recent experimental data on the magnonic nanofabric elements development and the results of numerical modeling and theoretical analysis on logic circuits engineering. We also provide the projected comparison with 45nm CMOS.

There are two basic components in the nanofabric: magneto-electric (ME) cells and spin wave buses. The ME cell is a magnetic element having at least two stable states for magnetization, which can be controlled by applying an electric field (e.g. using multiferroic heterostructures). ME cell is a multifunctional element aimed to convert electric signals into magnetic states and vice versa, store information encoded it the magnetization state, and to do data processing by changing its magnetization state as a function of the incoming spin wave signals. The communication among the ME cells is via the spin waves propagating through the ferromagnetic strips - spin wave buses [4]. There may be a number of spin waves simultaneously propagating in one spin wave bus. The overall change of magnetization in any part of the spin wave bus is a linear superposition of



A	B	C	Junction	Inverter
0	0	0	0	π
0	0	π	0	π
0	π	0	0	π
0	π	π	π	0
π	0	0	0	π
π	0	π	π	0
π	π	0	π	0
π	π	π	π	0

Fig.1 Schematics of magnonic NAND gate. There are three inputs (A,B,C) and the output D. The inputs and the output are the ME cells connected via the ferromagnetic waveguides –spin wave buses. The input cells generate spin waves of the same amplitude with initial phase 0 or π, corresponding to logic 0 and 1, respectively. The phase of the transmitted wave defines the magnetization of the output ME cell D. The Table illustrates the data processing in the phase space. The circuit can operate as NAND or NOR gate for inputs A and B depending the third input C (NOR if C=1, NAND if C=0).

multiple spin waves. Thus, the magnitude of the local magnetization change can be enhanced if the interfering waves come in phase, and it will be minimum if the waves interfere destructively (come with a π-phase shift). The latter provides a powerful tool for logic gate construction by exploiting spin wave buses as passive logic elements for spin wave phase modulation [5]. An example of the magnonic NAND gate is schematically shown in Fig.1. The gate consists of four multiferroic cells (three for inputs and one for the output). The input cells generate three input spin waves, which have 0 or π relative phase difference depending on the polarity of the applied voltage (e.g. +10mV corresponds to initial phase 0, and -10mV corresponds to initial phase π). The excited spin waves propagate through the spin wave buses and interfere at the point of junction. The phase of the transmitted wave corresponds to the majority of the interfering waves (e.g. the transmitted wave has phase 0 if two or three of interfering waves have initial phase 0). The length (composition) of the waveguides can be engineered in such a way to provide a certain time delay (phase shift) for the spin wave coming to the output ME cell. For example, if the length of the waveguide is an odd number of the wavelength, the output cell will be switched according to the majority of the input ME states. The cells will be switched to the opposite direction if the length of the waveguide is $\lambda/2$. The ability to control logic output by the signal phase provides a plethora of possibilities for logic gate construction.

The main contributions of this paper include the following: (i) An update on ME cell fabrication and testing, theoretical work on the ME cell integration with spin wave bus; (ii) experimental work on spin wave excitation and detection via ME cells; (iv) nano-scale fabric development including different logic circuit designs and projected comparison versus 45nm CMOS custom design. The rest of the paper is organized as follows. Section II presents the updates on ME cell development. We present proof of concept experimental data on spin wave excitation and detection in Section III. Different designs and comparison with CMOS are presented in Sections IV and V, respectively.

II. ME CELL DEVELOPMENT

ME cell is the element allowing for magnetization control by an electric field. In our work, we consider two possible approaches to ME cell construction. One of the approaches is based on use of synthetic multiferroics (SM) comprising piezoelectric and magnetostrictive materials, and the second one is based on the utilization of magnetic tunneling junctions (MTJ) exhibiting large voltage–controlled magnetic anisotropy (VCMA).

The schematics of the SM-ME cell are shown in Fig.2. The cell is composed of a piezoelectric single crystal substrate of $Pb(Mg_{1/3}Nb_{2/3})O_3]_{(1-.32)}$-$[PbTiO_3]_{.32}$ (PMN-PT) with either the (011) or (001) crystalline direction oriented normal to the surface, depending on the desired actuation scheme. As seen in Figs.2(A-B), the electrode configuration, the direction of the applied electric field, and strain response and magnitude depend on the type (i.e. crystal cut) of PMN-PT used. In the out-of-plane actuation scheme (Fig.2(A)), an (011) type PMN-PT substrate is actuated by an electric field through the thickness. Considerable in-plane anisotropic strains on the order of 1500ppm can be generated in this scheme [6]. By comparison, the in-plane actuation scheme (Fig.2(B)) has an electric field applied in-plane between two parallel electrodes which are deposited onto an (001) type PMN-PT substrate with etched side walls. Although more difficult to fabricate, this arrangement yields the highest possible anisotropic strains (on the order of 2500ppm) due to the significant difference between the d_{33} and d_{31} (d_{32}) piezoelectric coefficients.

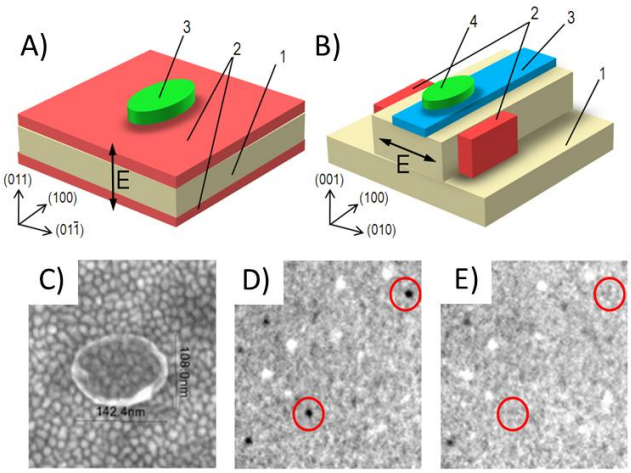


Figure 2: Schematics of two possible SM-ME cell configurations. (A) Out-of-plane actuation scheme with electric field applied through the thickness. 1. (011) PMN-PT substrate. 2. Thin film electrodes on top and bottom surface. 3. Ferromagnetic bit. (B) In-plane actuation scheme with electric field applied parallel to the surface. 1. (001) PMN-PT substrate with etched column structure. 2. Vertical sidewall electrodes. 3. Spin wave bus and/or insulating material. 4. Ferromagnetic bit. (C) SEM micrograph of 150x100x35nm^3 nickel ellipse on (011) PMN-PT substrate. B.) and C.) Photo Emission Electron Microscopy (PEEM) contrast images of magnetic bits on PMN-PT (011) under the 0 and 0.8MV/m electric field applied. Images by R. Chopdekar at the Paul Sherrer Institute, an ongoing collaboration with Mechanical and Aerospace Engineering Dept., UCLA.

In order to demonstrate a voltage-controlled magnetization switching, the arrays of 150x100x35nm^3 nickel elliptical bits were deposited onto 0.5mm-thick (011) PMN-PT substrate using an e-beam lithography and liftoff process. Fig.2(C) shows an SEM micrograph of a magnetic bit on the (011) PMN-PT substrate. An array of bits were imaged before and after the application of 400V (0.8M/m) to the substrate. As shown in Fig.2(D), the two bits circled in red show considerable magnetic contrast because their magnetization is perpendicular to the PEEM detector's axis of magnetic sensitivity. However, when an electric field of 0.8MV/m is applied to the substrate, the contrast in the bits is reduced considerably indicating that the magnetization of these bits has rotated approximately 90°.

The material structure of the VCMA-ME cell is shown in Fig.3. The multilayer is deposited at ambient temperature by magnetron sputtering onto a Si wafer with a thermal oxide layer. Following the

deposition, the multilayer is annealed at 300 °C for 2 hours in a 1 Tesla in-plane magnetic field that sets the direction of the exchange bias of the pinned layer. Subsequently, the multilayer is patterned into elliptical nanopillar shapes with the major and minor axis of 210 nm and 60 nm, the major axis being parallel to the direction of the exchange bias. Electric leads are

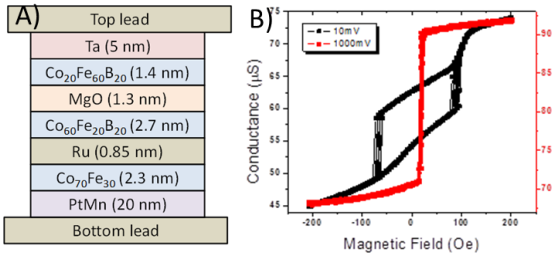


Fig. 3(A) Magnetic multilayer structure of a nanoscale magnetic tunnel junction for studies of voltage-induced switching of magnetization. (B) Conductance of the MTJ versus in-plane easy-axis magnetic field measured at applied voltage bias of 10 mV (black line) and 1000 mV (red line).

attached to the top and the bottom of the nanopillar for magneto-resistance measurements and studies of voltage-induced switching of magnetization.

In this structure, the thickness of the free layer (1.4 nm) is tuned to the range of in-plane to out-of-plane transition of magnetization arising from perpendicular surface magnetic anisotropy at the $Co_{20}Fe_{60}B_{20}$/ MgO and Ta/ $Co_{20}Fe_{60}B_{20}$ interfaces. At this thickness, the free layer magnetization's sensitivity to applied voltages is maximized, and there is a competition between in-plane and out-of-plane states of magnetization based on the minimization of the overall magnetostatic energy of the system. Two different states of the free layer magnetization give rise to two values of the MTJ nanopillar resistance. Black line in Fig.3 shows the conductance of the MTJ as a function of the in-plane magnetic field *H* measured at low voltage bias (10 mV) applied to the MTJ. The high and the low resistance states observed in the hysteresis loop of conductance versus magnetic field correspond to the two magnetization states in the free layer. Therefore, in-plane magnetic field can switch the free layer.

Application of a large positive voltage to the MTJ modifies the magnitude of perpendicular magnetic anisotropy at the $Co_{20}Fe_{60}B_{20}$/ MgO interface due to VCMA. This can be seen from the typical easy-axis hysteresis loop of conductance versus in-plane magnetic field (red curve in Fig.3) measured at V = 1000 mV. Quite remarkably, the high-bias (1000 mV) hysteresis loop exhibits coercivity that is much lower than that measured at low voltage bias (10 mV). This voltage control of the free layer coercivity enables switching of the free layer magnetization between two values of resistance by application of a positive voltage pulse to the MTJ.

We want to emphasis that in the both above-described ME structures the switching of magnetization is accomplish via by relatively small electric field, which, in turn, promises an ultra-low energy consumption for magnonic circuits [7].

In order to construct magnonic logic circuits, the ME cells should be coupled to the spin wave buses to excite and receive spin wave signals. The coupling can be accomplished via the exchange or dipole-dipole interactions among the spins of the ME cells and the spins of the spin wave bus. The main challenge with ME cell integration is associated with preserving the magnetic bistability of the ME cells, as the magnetic field produced by the bus may significantly reduce the energy barrier between the two states of magnetization. The geometry of the ME cell as well as the dimensions of the spin wave bus should be engineered to ensure a sufficient coupling without compromising ME cell's bistability. A possible schematics of ME cell integration with spin wave bus is shown in Fig.4(A). As a consequence of

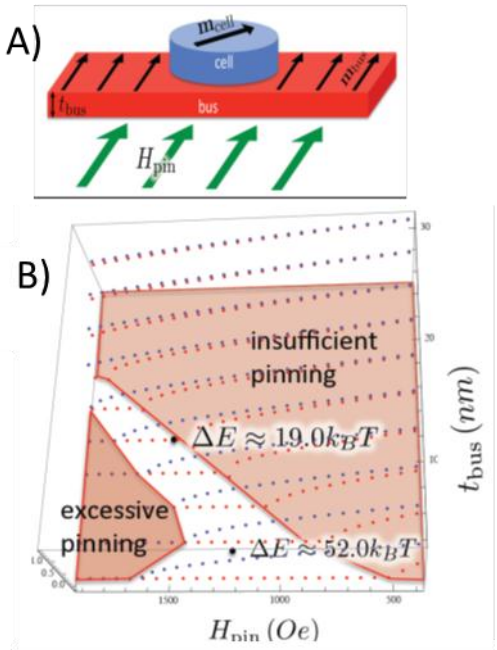


Fig.4 (A) Schematics of ME cell coupled to the spin wave bus via exchange interaction. (B) Results of modeling showing the region in parameter space preserving magnetic bistability of the ME cell. The locus of blue points represents the angular separation in radians of the bistable equilibria as a function of applied pinning field and bus thickness. The locus of nonzero red points represents bistability of the bus itself in the absence of coupling to the cell, indicating insufficient pinning by the applied.

the exchange coupling between the ME cell and the bus, the magnetization is continuous across the cell-bus interface, straining the magnetic texture in the bus near the cell. Lest the cell magnetization be pinned in one direction, the easy axis of the cell is oriented perpendicularly to the direction of magnetization in the bus far from the cell (which is taken to be either in the direction of the bus easy axis or to be pinned along the hard axis in the easy plane by a pinning field). The cell and the region of the bus directly below are assumed to be monodomain, whereas the magnetization in regions of the bus outside is obtained by solving the static equation of motion in the bus plane; with the boundary condition that magnetization in the bus is everywhere continuous, the bus magnetization away from the cell is therefore completely determined by the direction of the

monodomain cell. Last, to obtain the direction of the cell's magnetic moment, we express the total energy of the bus and cell magnetization as a function of this direction and search for a minimum. Generally, we find two equilibria for the cell magnetization, separated by an angle $\Delta\theta$ and energy barrier ΔE; when these vanish, bi-stability of the cell is compromised. In the first scenario, the bus magnetization lies along the easy axis in the absence of coupling to an ME cell; the cell must therefore be fabricated so that its easy axis is perpendicular to that of the bus. The angular separation $\Delta\theta$ of the cell equilibria now becomes a function of device parameters, e.g. the thickness and width of the bus, the thickness of the cell, etc. We find generally that bistability is compromised when the cell is too thin or the bus is too thick.

In the second scenario the bus magnetization is pinned along its hard axis by an applied field H_{pin}, and the cell is oriented so that its easy axis coincides with that of the bus. The applied field H_{pin} must be sufficiently strong so that the bus magnetization is pinned, but not strong enough that bi-stability of the cell is jeopardized. To verify whether or not the cell magnetization is pinned, we follow the approach outlined above and look for a finite angular separation $\Delta\theta$. Likewise, to determine if the bus is sufficiently pinned, we again minimize the energy (but without the contribution from the cell) as a function of the magnetization direction of the region below the cell; if there exists here a nonzero value of $\Delta\theta$, the applied field H_{pin} is insufficient to pin the bus magnetization. We find that there indeed exists a region in parameter space wherein the bus is pinned, but the cell is bistable, as we require.

Fig.4(C) shows the results of micromagnetic simulations, where ME cell stability was calculated for different cell thicknesses and magnetization values. These results unambiguously show that thermally robust bistability of the cell magnetization ($\mathbf{\Delta E}$~100 k_BT) is possible under suitable choice of parameters and is improved as the cell thickness and saturation magnetization are increased while the bus thickness and saturation magnetization are decreased.

III. Spin Wave Excitation and Detection via ME Cells

The information transfer within the nanofabrics is via spin waves, where ME cells serve as generators and recipients of the spin wave signals. Fig.5 shows the test structure comprising SM-cells and micro-antennas aimed to demonstrate the feasibility of spin wave generation and detection by ME cells. This structure allows us to generate spin wave by the ME cell and detect the excited wave by the micro-antenna, and vice versa, use ME cell as a detector for spin waves excited by the micro-antenna. The structure includes a 40 nm thick Ni/NiFe bi-layer (20nm/20 nm) patterned in a 4um wide and 200um long bar (spin wave bus) on the top of the PMN-PT substrate with (001) crystal orientation. The material of the bar was chosen to provide both low loss medium for spin wave propagation (NiFe) and magnetostrictive properties for strain induced anisotropy change (Ni). A radio-frequency voltage was applied to a micron-scale confined region of the PMN-PT substrate underneath ferromagnetic bar (ME cell) to excite spin-waves by rapid anisotropy change due to the local voltage induced strain. The measurements were performed by using a two port vector network analyzer simultaneously detecting reflected and transmitted signal components.

Figs.5(B-C) show the experimental data on spin wave excitation and detection by ME cell. The color

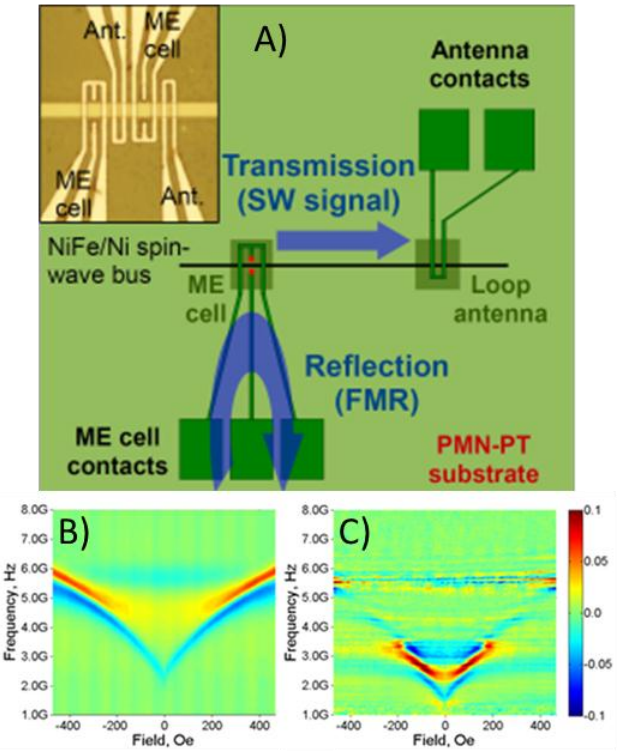


Figure 5. (A) Schematic of the test setup for two port measurements between conventional loop antenna and SM-ME cell. (B) Spin wave generated by ME cell/detected by the antenna. (C) Spin wave generated by the antenna/detected by ME cell. All measurements at RT.

plots show the transmitted amplitude as a function of frequency and the fixed bias magnetic field. The propagating spin waves were detected at distances as far as 40 um. To verify the spin wave origin of the detected signal, all experiments were carried out at different bias magnetic field from -500Oe to 500 Oe applied along hard-axis of the spin wave bus. The obtained data clearly confirm the feasibility of using ME cells for spin wave generation and detection. All measurements were performed at room temperature.

IV. Magnonic Spin Wave Functions (SPWFs) Logic Design

Generally, CMOS logic circuits are implemented using Boolean gates (e.g. AND/OR) based on SOP or

POS realizations. In this approach, 2-input or 3-input standard gate libraries are constructed and larger circuits are built by cascading a large number of these elementary gates. However, it is well known that such a logic design approach, has two major drawbacks, i) exponential degradation in performance is observed for high fan-in, ii) Leads to inefficient implementation with large number of logic levels and gates.

Several alternate logic styles have been proposed to overcome the drawbacks of the conventional Boolean logic. One of the popular alternatives is based on threshold/majority logic. Threshold gates fundamentally realize more complex logic functions compared to conventional Boolean gates (AND, OR etc.); consequently, reducing the number of logic levels and the overall gate count required to realize a given circuit [8,9].

However, since the physical implementations (e.g. CMOS based) of the threshold gates are known to be highly complex, this logic style has had little impact on CMOS VLSI design. Moreover the fan-in for majority based implementations is generally limited to 3 or 4. Several algorithms have been proposed for designing high fan-in majority gates using 3-input majority gates [10]. This multi-level implementation further increases the implementation complexity.

On the contrary, SPWFs leverage on the wave interference phenomenon and thus no special gate/component is required to realize the majority function. Moreover, since wave amplitude can also be used for information encoding, data on multiple waves can be represented in a compressed manner using only single (or few) wave. This significantly improves overall circuit implementation efficiency. In this work, we have explored the benefits of such compressed data representation in SPWF based parallel counters.

A. SPWF-Based Parallel Counters

Parallel counters are digital circuits with 'n' inputs and '$\log_2(n+1)$' output bits representing the number of 1's in the 'n' input bits set [11,12]. Generally, parallel counters are used in the realization of fast parallel multipliers. SPWF-based parallel counter designs and relevant comparisons vs. 45nm CMOS are shown next.

Fig. 6, Fig. 7 and Fig. 8 show possible implementations for SPWF based (3,2), (7,3) and (15,4) parallel counter designs respectively. A (3,2) parallel counter has 3 inputs (A_2, A_1, A_0) and 2 outputs (O_1, O_0) which implements the following logic functions:

$$O_1 = MAJ(A_2, A_1, A_0)$$

$$O_0 = MAJ(A_2, A_1, A_0, -2MAJ(A_2, A_1, A_0))$$

It can be observed from Fig. 6 that the resultant wave (W_3) at output O_1 (MSB) implements a simple majority function of input spin waves generated by A_0, A_1 and A_2. The resultant waves W_4 & W_5 encode information in both phase and amplitude, thus enabling a compressed data representation. This

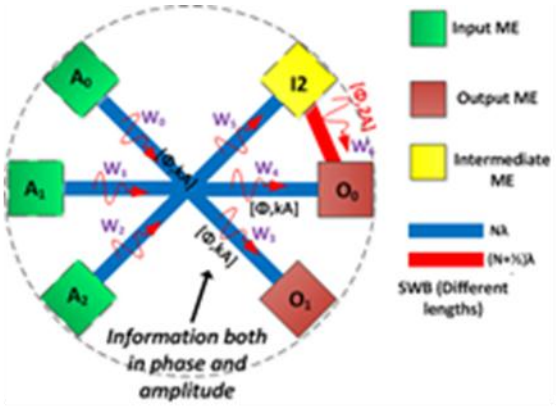


Fig. 6: SPWF layout of (3,2) parallel counter. Here, waves W3, W4 and W5 encode information both in wave phase and amplitude leading to compressed information representation.

feature simplifies implementing O_0 by reusing these resultant waves, instead of duplicating the primary inputs. The intermediate cell I2 in Fig.6 latches the incoming wave (W_5) and generates an outgoing wave (W_6) of *fixed amplitude*, which is inverted through layout ([n+1/2)λ] waveguide) to implement '-*2MAJ*(A_2,A_1,A_0)'.

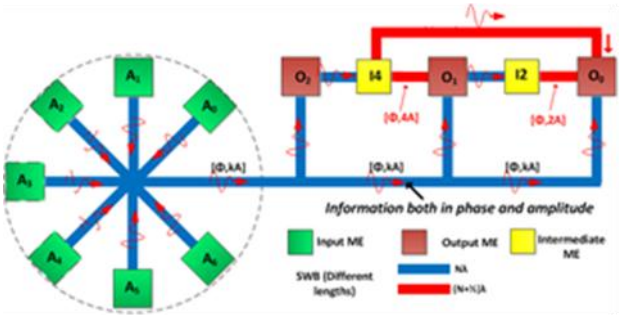


Fig. 7: SPWF layout of (7,3) parallel counter.

The (7,3) and (15,4) counters are also implemented using similar majority logic functions. Compressed data representation leads to significant logic complexity reduction compared to corresponding CMOS designs. For comparison, 45nm NANGATE standard cell library based (7,3) counter design is shown in Fig. 9. This design uses several levels of logic and over 100 transistors vs. only 12 ME cells in the corresponding SPWF layout (Fig. 7).

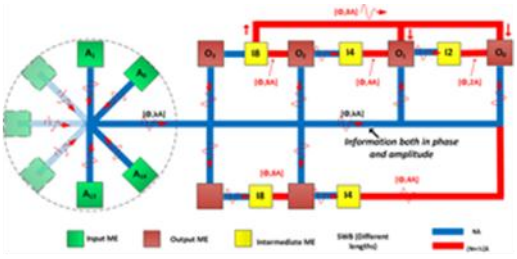


Fig. 8: SPWF layout of (15,4) parallel counter.

V. Comparisons vs. 45nm CMOS

SPWFs-based designs were evaluated based on the layout shown in Figures 6-8. Here, ME cells dimension is assumed to be 100nm*100nm with a switching delay of 100ps. Performance is based on critical path analysis, which includes ME cell switching delay and wave propagation delay along the critical path. Spin wave group velocity is assumed to be 10^4m/s for calculating spin wave propagation delay. Since spin wave propagation does not involve physical movement of charge particles, power estimations for SPWFs designs are mainly based on ME cell switching activity. Based on data from numerical simulations and by using a simple capacitor approximation, ME cell switching energy is estimated to be as low as 10aJ [7].

CMOS evaluations were obtained by mapping the designs to 45nm NANGATE standard cell libraries using Synopsys Design Compiler tool. Table 1 shows the projected comparisons of SPWF design vs. CMOS.

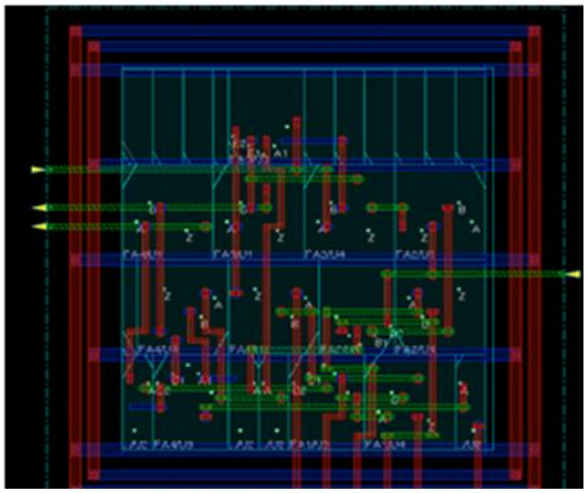


Fig. 9: CMOS (7,3) parallel counter implementation based on 45nm NANGATE standard cell libraries.

Projected comparisons show that up to 40X power reduction and 53X area reduction can be expected with comparable performance for SPWF-based (3,2) parallel counter. Moreover, as SPWFs enable efficient high fan-in logic realization, even higher benefits can be expected with higher order parallel counters. For the (15,4) parallel counter, up to 90X power reduction and about 103X area reduction can be expected with approximately 1.36X performance benefit. These results show that magnonic circuits based on SPWF logic provides several advantages over conventional charge based electronics that could lead to game changing nanoscale systems in the future

Table 1: Comparison of SPWF vs. 45nm CMOS parallel counters.

CMOS			
	Area (μm^2)	Delay (ps)	Power (μW)
(3,2) Counter	8	280	6
(7,3) Counter	27	740	14
(15,4) Counter	72	1200	27
SPWF			
	Area (μm^2)	Delay (ps)	Power (μW)
(3,2) Counter	0.15	350	0.15
(7,3) Counter	0.2	670	0.2
(15,4)	0.7	880	0.30

VI. Conclusions

Spin wave nanofabric offers a promising route to beyond CMOS logic by taking the advantages of using magnetization as a state variable and spin waves for information transmission and processing. On one hand, the use of magnetic states for information storage allows us for building non-volatile circuits with zero static power dissipation. On the other hand, the utilization of phases in addition to amplitudes makes it possible to enhance logic functionality and significantly reduce the number of components per circuit compare to the conventional approach. Major accomplishments during the past year include the successful demonstration of the nanofabric components (i.e. ME cells development) and the advances in spin wave logic functions design. For the first time, it was experimentally demonstrated spin wave excitation by ME cell attached to the spin wave bus. It is important to note, that the electric field required for high frequency spin wave excitation (up to 5 GHz) does not exceed the previously reported value of 1MV/m [7]. The latter confirms our projections on the ultra-low active power consumption in multiferroic-based circuits. More than that, it was also observed spin wave signal detection by the ME cell at the distances up to 40um away from the excitation point. The obtained experimental data demonstrate the practical feasibility of spin wave nanofabric implementation. The estimates on the magnonic logic circuits performance predict significant advantage over the scaled CMOS (i.e. ~40X power reduction and 53X area reduction for (3,2) parallel counter). Even higher benefits are expected for more complex logic circuits. In future, we plan to continue our work towards the practical demonstration of a complete logic circuit (i.e. 1-bit Adder) and experimentally validate the expected advantages of the spin wave approach.

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