Integrated Nanowire Systems for Post-CMOS Computing

Mostafizur Rahman*, Pritish Narayanan and Csaba Andras Moritz
Electrical and Computer Engineering, UMass Amherst
{rahman, andras}@ecs.umass.edu

Abstract

CMOS faces new device and technology challenges: MOSFETs require ultra-sharp doping profiles and complex processing; integration of devices into circuits requires arbitrary interconnection with overlay precision beyond known manufacturing solutions ($3\sigma=\pm3nm$, 16nm CMOS, ITRS'11[1]). To overcome these challenges, we propose a new nanoscale computing fabric with integrated design of device, interconnect and circuits to minimize manufacturing requirements while providing ultra-dense, high-performance, and low-power solution surpassing scaled CMOS. Devices with uniform doping profiles, regular arrays tolerant to mask misalignment and novel circuits with limited customization are discussed. Device evaluations prove that proposed devices simplify manufacturing complexity vs. CMOS while being competitive ($I_{ON} = 14\mu A$, $I_{ON}/I_{OFF} > 10^6$). Simulations show 100% yield at overlay imprecision as high as $3\sigma=\pm8nm$ (manufacturing solutions known, ITRS'11[1]). Benchmarking of processor design vs. equivalent 16nm CMOS shows 3x density, 5x power benefits at comparable performance. Memory benchmarking shows 35x leakage power, 3x performance improvement over 16nm SRAM.

I. Introduction

CMOS faces many new manufacturing challenges with scaling of technology nodes. For example MOSFET devices require ultra-sharp source and drain junctions with abrupt doping profiles and complex fabrication steps [2] with precise annealing and spacer techniques. Careful sizing is required to meet noise/performance requirements. Integration of devices into circuits require arbitrary interconnections at nanoscale precision, implying very stringent overlay alignment requirements ($3\sigma=\pm3nm$ for CMOS 16nm node [1]).

In this paper we propose a post-CMOS computing technology (or nano-fabric) that overcomes many of the device customization and integration challenges faced by CMOS while at the same time achieving area/power/performance benefits. As opposed to creating individual devices on a substrate and interconnecting them into arbitrary layouts, we propose regular layouts with integrated assembly of devices and local interconnects as part of the fabric itself. Furthermore, new simplified devices (called Metal-Gated Junctionless Nanowire Field Effect Transistors, or MJNFETs) that do not require differently doped regions in close proximity or high thermal budgets are used. New circuit styles without complementary FETs or arbitrary sizing requirements also simplify manufacturing.

We present the overall fabric organization, and a layer-by-layer assembly sequence that achieves integrated devices as part of the overall fabric. We show through overlay simulations that 100% yield is obtained even for overlay misalignments as high as $3\sigma=\pm8nm$ (manufacturing solutions known, ITRS 2011 [1]). We present the MJNFET structure, and validate its behavior through detailed Synopsys Sentaurus process and device simulations. We show the device to have a threshold voltage of 0.3V, and on/off current ratio of $> 10^6$, which meets circuit requirements. Finally, we show examples of logic and volatile memory circuits implemented with single-type MJNFETs and verify their behavior through circuit simulations. Benchmarking results show up to 35x leakage power reduction, and 3x performance benefit for a volatile memory design vs. 16nm scaled SRAM, and 3x density and 5x total power benefits for a processor design vs and equivalent 16nm CMOS implementation.

The rest of the paper is organized as follows: Section II describes the overall fabric organization; MJNFET device and device simulation results validating their behavior are discussed in Section III; Section IV presents the integration approach and simulations that prove simplified overlay requirements for our fabric; Section V provides examples of logic and volatile memory circuits mapped to the fabric and detailed benchmarking vs. CMOS; and Section VI concludes the paper.

II. Physcial Fabric Overview

In the CMOS manufacturing flow, individual devices are first created on a substrate, followed by arbitrary interconnections through metal stacks to form functional circuits. Given the scaling of feature sizes below 32nm and the arbitrary placement requirements for devices, extremely precise overlay alignment is required ($3\sigma=\pm3nm$ [1]) for integration. By contrast, we present new nano-fabrics with integrated devices and interconnects that are part of the fabric itself, and do not require explicit local interconnection of devices post-fabrication. Furthermore if the defined patterns are regular (e.g. parallel arrays), lithographic masks may be offset over the array without yield loss.

Fig. 1 shows the overall vision for our proposed physical fabric, called Nanoscale 3-D Application Specific Integrated Circuits (N^3ASICs). It consists of regular arrays of patterned semiconductor nanowires, called tiles. Integrated devices and local interconnects are achieved on the nanowires themselves, without the need for fine-grain arbitrary routing. 3-D metal

routing is required only at inputs and outputs (at tile-level granularity). Orthogonal metal gates carry input signals. Outputs are routed through vias and metal layers to subsequent tiles. Logic and memory circuits can be implemented on these tiles (Examples in Section V). In keeping with the simplified manufacturing mindset, customization of circuits is limited to defining the positions of nanowire crosspoint devices, and does not require arbitrary sizing or complementary doping types. In the next section, we will describe novel junctionless device structures that can be integrated into the N3ASICs fabric further simplifying manufacturing requirements.
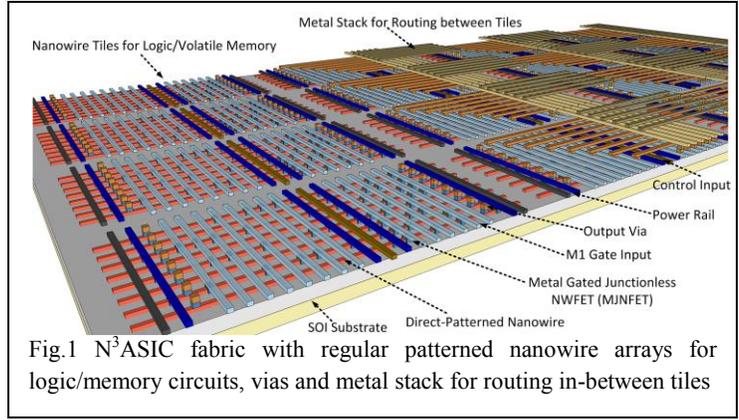

Fig.1 N^{3}ASIC fabric with regular patterned nanowire arrays for logic/memory circuits, vias and metal stack for routing in-between tiles

III. Metal-Gated Junctionless Nanowire FETs (MJNFETs)

Conventional inversion-mode CMOS devices require ultra-sharp source-channel and drain-channel junction with dopant concentrations changing several orders of magnitude within a span of 1nm-2nm [3]. Achieving this requires extremely complex and precise control of spacer techniques and high temperature annealing processes. In this section, we propose and describe Metal-gated Junctionless Nanowire FETs (MJNFETs) that are fully compatible with the N^{3}ASICs fabric and provide significantly reduced manufacturing complexity vs. CMOS.

The device structure is shown in Fig. 2A. It consists of a uniformly doped channel nanowire without drain- or source-junctions, a high-κ dielectric material, and an orthogonal metal gate. MJNFETs operate on the principle of channel depletion induced by work-function difference between the metal gate and the doped channel. Given the nanoscale dimensions of the channel cross-section, the channel region can be completely depleted of carriers at zero gate voltage, leading to normally OFF devices. Applying a voltage bias on the metal gate eliminates the work-function difference, turning ON the device.

MJNFET device behavior was studied through detailed 3-D Synopsys Sentaurus process and device simulations. The device structure was created using process simulations [4] considering detailed process effects such as implantation parameters, diffusion temperature, oxide deposition rate etc. For device simulations, hydrodynamic charge transport model with quantum corrections [5] was used to model charge transport accounting for quantum confinement effects. Simulated device dimensions were 16nm (gate length) X 10nm (channel width) X 10nm (channel thickness). HfO$_2$ gate dielectric with 2nm thickness and Nickel (workfunction = 5eV [6]) gate was assumed. N-type Si nanowire channels were simulated with a sufficiently high doping (2 X 10^{19} dopants/cm^3) to achieve a high on-current.

Results of Id – Vg simulations (Fig. 1B) validate the expected behavior of MJNFETs. At zero gate voltage, drain current is in the order of ~10pA implying a normally OFF condition. As a positive bias is applied, carriers are accumulated into the channel. Above the threshold voltage a conducting path is established and the device is considered ON. Accumulation increases up to the flat-band condition, when the channel concentration reaches the initial doping concentration. ON-current
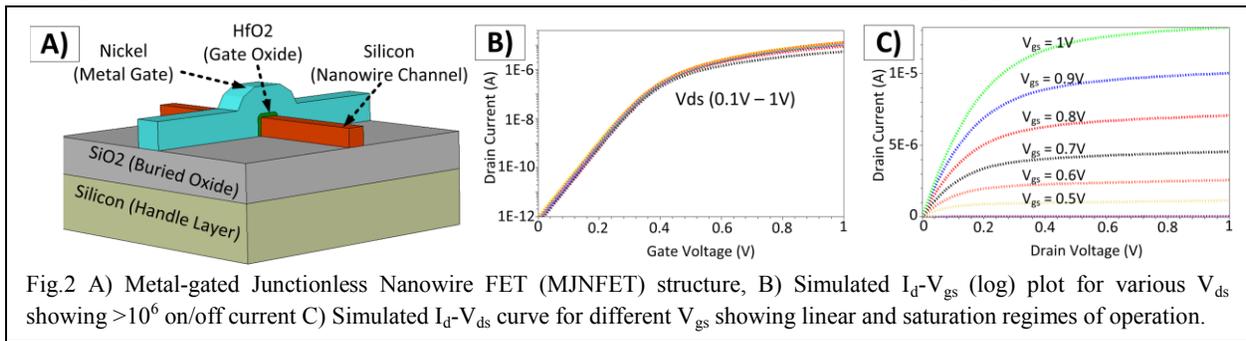

Fig.2 A) Metal-gated Junctionless Nanowire FET (MJNFET) structure, B) Simulated I$_d$-V$_{gs}$ (log) plot for various V$_{ds}$ showing >10^6 on/off current C) Simulated I$_d$-V$_{ds}$ curve for different V$_{gs}$ showing linear and saturation regimes of operation.

for this device was found to be 14μA. Fig. 2C shows linear and saturation regimes of operation similar to N-type FETs. These results show that the MJNFET with simplified manufacturability is still competitive against conventional NMOS (PTM [7] 16nm NMOS: 15μA I_{ON}). Furthermore, in MJNFETs using a metal gate implies that doping requirements are ameliorated compared to even previous junctionless structures [3] which need different doping types on gate and channel regions.

IV. Fabric Integration and Overlay Requirements

N^{3}ASICs fabrics with MJNFETs can be assembled using a bottom-up integration sequence (Fig. 3) that combines unconventional patterning and photolithography steps while carefully managing overlay requirements. Unconventional patterning approaches (e.g. Nano-imprint lithography (NIL) [8]) can achieve very high density nanowire-arrays, but suffer from extremely poor overlay alignment. Therefore, in our approach, a single *a priori* unconventional patterning step (without any registration requirement) is carried out to define high-density regular nanowire arrays (Fig. 3B). All subsequent steps use conventional lithography. Gate oxide and metal are deposited at nanowire FET cross-point locations (Fig. 3C). This step achieves simultaneous formation of devices and local interconnections on the patterned nanowires, with self-aligned depletion of channel regions under deposited gates.
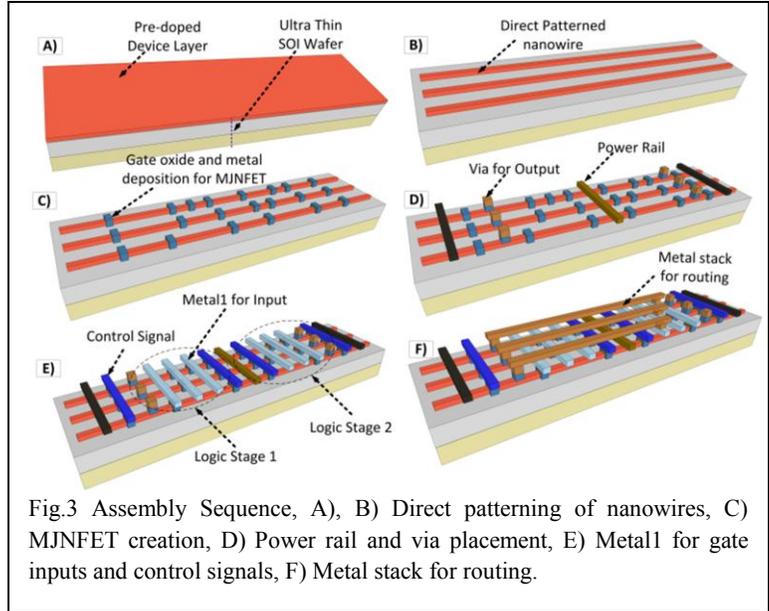

Fig.3 Assembly Sequence, A), B) Direct patterning of nanowires, C) MJNFET creation, D) Power rail and via placement, E) Metal1 for gate inputs and control signals, F) Metal stack for routing.

Vias for tile input/output, power rails (Fig. 3D) and metal routing layers (Fig. 3E, 3F) are subsequently created. This approach thus achieves 3-D integration without any special manufacturing requirements while ensuring finer nanoscale resolution (and consequently higher density) than can be achieved with lithography at the bottom. This integration sequence also highlights the significant reduction in doping requirements: given a uniformly doped SOI substrate, no additional doping steps are required in the assembly sequence.

Overlay simulations based on the methodology proposed in [9] were carried out to determine overlay limited yield. Briefly, overlay misalignment between successive masks were modeled

Fig.4. Yield vs Overlay misalignment for N^{3}ASIC fabric

as Gaussian random variables, and Monte Carlo simulations were carried out in a custom simulator to determine the number of functioning chips. The simulations were carried out for 3σ overlay misalignment values projected by ITRS. The results (Fig. 4) show that close to 99% yield may be obtained for $3\sigma=\pm9$nm overlay (manufacturing solutions known as per ITRS'11 [1]) for uniform nanowire arrays with 32nm pitch (equivalent to 16nm CMOS technology node). Fig. 4 shows that even with a pessimistic mask overlay projection of $3\sigma=\pm16$nm a yield of 83% can be observed. These overlay requirements are far less stringent than the requirement for 16nm CMOS ($3\sigma=\pm3$nm for 16nm CMOS, ITRS'11[1]).

V. Logic and Volatile Memory Implementation

N^{3}ASICs use a novel dynamic circuit style with single-type FETs that is amenable to implementation on regular array fabric layouts. This circuit style does not require complementary devices, or arbitrary placement and sizing. In this section, we provide examples of logic, memory circuits on N^{3}ASIC fabric using these circuit styles and discuss benchmarking results.

Fig. 5A shows a 1-bit full adder implementation on the N^{3}ASICs fabric; Fig. 5B shows the equivalent circuit schematic. This implementation uses a cascaded 2-level NAND-NAND logic style with dynamic circuits[10][11]. All devices are identical and do not require sizing/doping. Inputs are received on vertical metal wires (M1) of the left tile; minterms are generated at the outputs of this tile and through vias and M2 wires, are routed to the inputs of the second tile; carry and sum outputs of the adder are generated at the output vias of the second tile. These outputs may be cascaded to subsequent stages using the metal stack. HSPICE circuit simulations validate circuit functionality (Fig. 5C).

Fig. 5D and 5E show fabric and circuit schematics of a 10 Transistor Quasi-Static Nanowire RAM (10T - NWRAM) [12]. This circuit implements cross-coupled volatile memory without the need for complementary devices or careful sizing of FETs required in SRAM. True and complementary information bits are stored in cross-coupled dynamic NAND gates, and separate access signals are used for read/write. The 10T-NWRAM shares features of both static (cross-coupled) and dynamic (circuit style, restore) volatile memory, but with better performance than SRAM. HSPICE circuit simulations validating volatile memory behavior are shown in Fig. 5F.
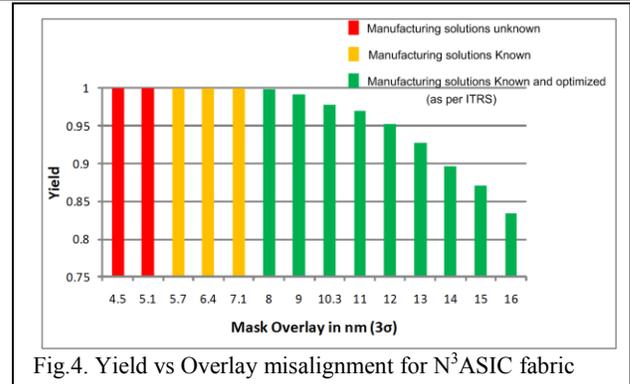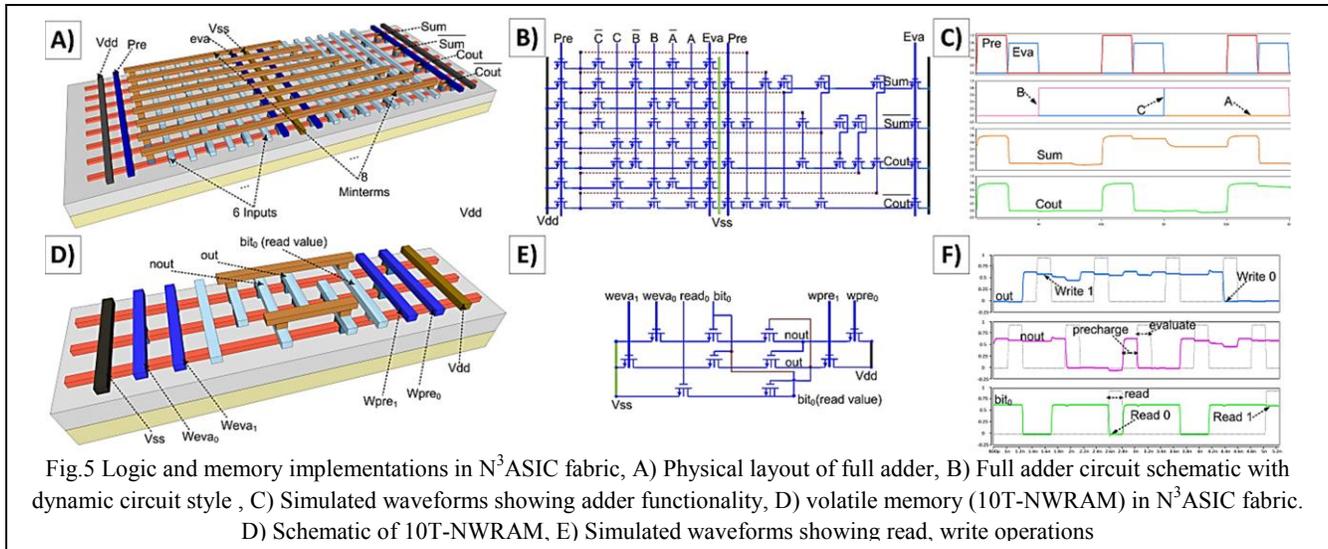
Fig.5 Logic and memory implementations in N^{3}ASIC fabric, A) Physical layout of full adder, B) Full adder circuit schematic with dynamic circuit style , C) Simulated waveforms showing adder functionality, D) volatile memory (10T-NWRAM) in N^{3}ASIC fabric. D) Schematic of 10T-NWRAM, E) Simulated waveforms showing read, write operations

Benchmarking of N^{3}ASIC logic (a processor design, WISP-0 [13]) and volatile memory circuits (10T-NWRAM) vs. equivalent 16nm CMOS designs was done to quantify benefits. PTM device, interconnect models [7] were used in CMOS simulations. Physics based device simulation models were used for nanowire FETs. Interconnect dimensions for CMOS and N3ASICs was determined by lithography design rules. Results are summarized in Tables I & II. For a processor design, the N3ASICs fabric was shown to be 3X denser, and 5X more power efficient than the equivalent 16nm CMOS (Table I). The 10T-NWRAM was shown to have 35X less leakage and 3X performance with comparable area and active power consumption (Table II). These results prove that using a combination of device, circuit and integration choices, novel nano-computing systems can be designed with reduced manufacturing complexity and area/power/performance benefits over scaled CMOS technologies.

Table I. Comparison of N^{3}ASIC vs CMOS for WISP-0 Processor

16nm Technology node	N^{3}ASIC WISP-0 Processor	CMOS WISP-0 processor
Area (μm^2)	22	66.24
Performance (*GHz*)	6.32	6.25
Power (μW)	14.36	77.9

Table II. Comparison of 10T-NWRAM vs scaled CMOS SRAM

16nm Technology node	10T-NWRAM Cell	Scaled CMOS SRAM cell
Area (μm^2)	0.037	0.033
Active Power *(nW)*	2.83	1.47
Standby Power *(μW)*	0.44	15.6
Read Time *(ps)*	8.51	25.9

VI. Conclusions

A new computing fabric was introduced that addresses device, interconnect and integration synergistically to simplify critical manufacturing challenges facing CMOS. Manufacturing complexity was reduced at all design levels while still achieving benefits vs. equivalent CMOS designs. Regular array-based fabrics with devices and interconnect created together simplify overlay precision required. Simulations show that 100% yield can be obtained with overlay precision available with present-day systems (3σ=±8nm). MJNFET devices with uniform doping profiles reduce device doping requirements while still providing competitive device metrics with 14μA I_{ON} and $I_{ON}/I_{OFF} > 10^6$. Benchmarking of a N^{3}ASICs processor design vs. an equivalent 16nm CMOS implementation shows 3x density, 5x total power benefits at comparable performance. Benchmarking of 10T-NWRAM vs 16nm CMOS SRAM show 35x leakage reduction and 3x performance improvement.

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