Validating Cascading of Crossbar Circuits with an Integrated Device-Circuit Exploration

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Abstract **We present an integrated approach that combines 3D modeling of nanodevice electrostatics and operations with extensive circuit level validation and evaluation. We simulate crossed nanowire field-effect transistor (xnwFET) structures, extract electrical characteristics, and create behavioral models for circuit level validations. Our experiments show that functional cascaded dynamic circuits can be achieved by optimal selection of device level parameters such as V_{TH}. Furthermore, V_{TH} tuning is achieved through substrate biasing and source and drain junction underlap, which does not pose difficult manufacturability and customization challenges. Circuit level simulations of up to forty cascaded stages show correct propagation of data and adequate noise margins.**

***Index Terms*— NASICs, Semiconductor Nanowires, Device Characterization, Field Effect Transistors, Dynamic Circuits**

I. Introduction

Nanoscale computational fabrics have to overcome challenges at various design levels, including manufacturing, devices, circuits and architecture, and fault tolerance. Therefore design choices at individual levels need to be compatible with the fabric as a whole. For example, in addition to having the requisite electrical characteristics, nanodevices should i) meet circuit requirements and function as expected and ii) not require extensive customization that poses insurmountable challenges to non-conventional manufacturing process.

In this paper we explore devices and circuits for a nanoscale fabric in a tightly integrated fashion, with simulations at the circuit level built on accurate 3-D device simulations of the electrostatics and operations. We extract the *I-V* characteristics and capacitances for various device structures. We then create behavioral models of this data for a circuit simulator and use these to validate circuit style and functionality. We also discuss implications of device choices on manufacturing. While this work is focused on crossed nanowires (NW) field-effect transistors (FETs) for the NASIC (Nanoscale Application Specific Integrated Circuits) computational fabric [1][2][3][4], the approach and methodology are fairly generic, and can be applied to other devices and computational fabrics.

NASICs are built on regular 2-D semiconductor nanowire grids with crossed nanowire field-effect transistors (xnwFET) and dynamic circuit styles. While dynamic circuit styles for the NASIC fabric have been extensively explored in [1][4], this is the first time that co-design of devices and circuits has been accomplished by using accurate physics based 3D device models. Accurate modeling is especially important for the latest dynamic circuits with single-type FETs [4], where using only *n*-type devices simplifies manufacturing requirements and improves performance, but may lead to reduced noise margins.

We explore different devices and show how the optimal choice of device parameters such as V_{TH}, I_{ON}/I_{OFF} ratios etc. enables correctly functioning cascaded dynamic circuits. Importantly, we also discuss how these device level characteristics can be achieved without unrealistic customization requirements on the manufacturing process.

The main contributions of this paper are: i) a generic methodology for integrated device-circuit explorations of nanodevice based systems is presented ii) physics based accurate 3D characterization of xnwFET behavior is shown and iii) nanowire crossbar circuits are explored with different nanodevices and NASIC dynamic circuit style is validated.

The rest of the paper is organized as follows. A brief overview of NASICs with an emphasis on device requirements and circuit styles is shown in Section I. Section II describes the methodology for integrated device-circuit exploration. Section III presents device simulation experiments and results. NASIC single-type FET dynamic circuit validation for different devices is presented in section V. Section VI discusses manufacturing implications. Section VII concludes the paper.

II. Overview of NASICs

Semiconductor nanowires have been demonstrated with a variety of materials including silicon [5][6], germanium [7][8], InSb [9] etc. By using non-conventional assembly techniques [10][11][12], it may be possible to assemble these materials

We acknowledge support from the Focus Center Research Program (FCRP) - Center on Functional Engineered Nano Architectonics (FENA)..

into regular arrays and grids.

The NASIC fabric is built on these types of 2-D semiconductor nanowire grids with crossed nanowire field-effect transistors at certain crosspoints. The channel of a xnwFET is aligned along one NW while the perpendicular NW above it acts as gate. A typical xnwFET behavior has been reported in Silicon NWs in [13].

Fig. 1 shows an example of a NASIC circuit that implements a 1-bit full adder. This includes a semiconductor nanowire grid with peripheral microwires (MW) that carry V_{DD}, V_{SS} and dynamic control signals. xnwFETs are shown at certain crosspoints in the diagram. Channels of xnwFETs are oriented horizontally on the left plane, and vertically on the right. Inputs are received from vertical nanowires in the left plane. These act as gates to horizontal nanowire FETs implementing one stage of a dynamic circuit. The output of horizontal nanowires acts as gate to the next set of transistors whose channels are aligned in the vertical direction (right NAND plane). Multiple such NASIC tiles are cascaded together to form more complex circuitry such as microprocessors [1] and image processing systems [14].

All crossed nanowire devices used in the logic portions of the circuit are identical with no arbitrary doping or sizing requirement. Customization of the grid is limited to defining the positions of transistors. Furthermore, NASICs use a single doping type in all xnwFETs to reduce manufacturing requirements and improve performance [4].

NASICs use a dynamic circuit style with control signals driven from external reliable CMOS circuitry. Control signals coordinate the flow of data through NASIC tiles: horizontal and vertical signals are different, supporting cascading. Fig. 2 shows a typical NASIC control scheme but other schemes are also possible. Horizontal nanowire outputs are initially

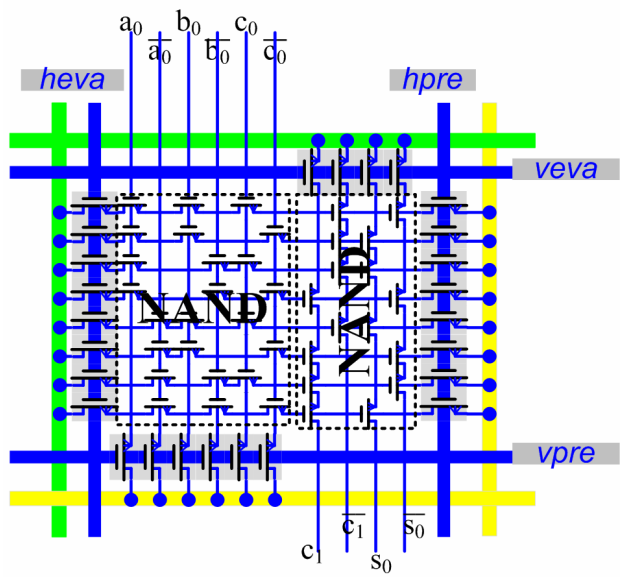

Figure 1. 1-bit dynamic NASIC full adder using NAND-NAND cascaded 2-level logic. Arrows show propagation of data through the tile. Thicker wires represent microwires and thin ones are nanowires. FETs shown on certain crosspoints.

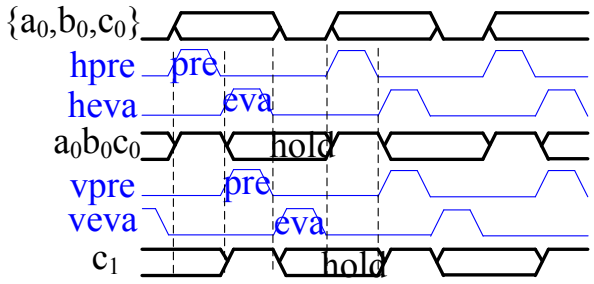

Figure 2. Dynamic control scheme in NASIC Designs

precharged to logic '1' by asserting *hpre*. *hpre* is then switched off and *heva* is asserted to evaluate inputs. Vertical nanowires are simultaneously precharged (*vpre* is asserted). In the next phase, both *hpre* and *heva* are switched off, and the horizontal nanowires are in 'hold' phase, during which time *veva* is asserted and outputs from the tile are evaluated. It implements implicit latching of the nanowire output after evaluation without the need for expensive flip-flops, and is essential for cascading multiple nanowire stages.

Integrating accurate physics based device models with circuit level evaluations can validate NASIC dynamic circuit concepts and cascading. Furthermore, other effects such as the noise margin impact of using *n*-type xnwFET for pull-up can be analyzed from a circuit perspective.

III. Methodology for Integrated Device and Circuit Exploration

This section details the methodology used for integrated nanodevice-circuit explorations. Results from individual steps will be presented in subsequent sections of the paper.

Device level characterization of xnwFET structures is done using 3D simulations on the Synopsys Sentaurus device simulator [15]. Drain current vs. gate voltage (transfer) characteristics are obtained for drain voltages varying between 0.01V to 1.0 V, which covers the operating range of the devices in the NASIC dynamic circuits. Gate-source and gate-drain capacitances are also extracted as a function of the gate voltage. Regression analysis is carried out on the drain current data, and multivariate polynomial fits (for FET on-region behavior) and exponential fits (for off-region behavior) are extracted using DataFit software[1]. These relationships express the drain current as a function of two independent variables, gate-source (V_{GS}) and drain-source (V_{DS}) voltages. These fits are then incorporated into subcircuit definitions for voltage-

[1]A Note on Regression-based vs. Analytical Modeling: A regression based approach is very generic and can be used to fit arbitrary device characteristics. Coefficients extracted from regression data fits are representative of the device behavior over sweeps of drain-source and gate-source voltages. This is in contrast to conventional in-built models in SPICE for MOSFETs and other devices, which use analytical equations derived from theory and physical parameters such as channel length and width. The regression coefficients in our approach may not directly correspond to conventional physical parameters. Therefore different regression fits will need to be extracted for devices with varying geometries, doping etc.

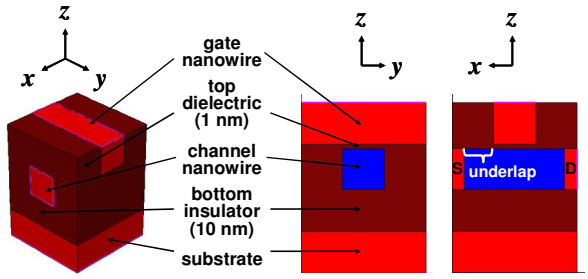

Figure 3a. Si CNWFET structure used in our 3D simulations. The channel nanowire is *p*-type (blue) and the gate/source/drain/substrate region are *n*-type (red).

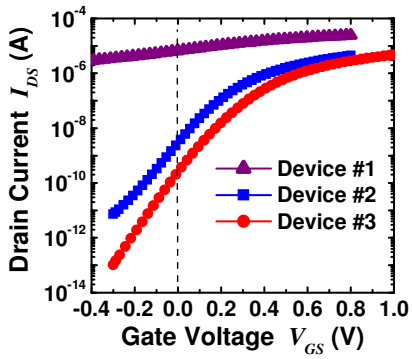

Figure 3b. Simulated transfer characteristics of xnwFETs with parameters listed in Table I.

controlled resistors in HSPICE [16]. Capacitance data from Sentaurus is directly integrated into HSPICE using voltage-controlled capacitance (VCCAP) elements and a piece-wise linear approximation since only small variations in capacitance were observed with V_{GS} increments. The regression fits for currents together with the piece-wise linear model for capacitances and subcircuit interconnections define the behavioral model for xnwFET devices used in circuit simulation.

Once behavioral data has been incorporated into HSPICE, multiple experiments are conducted including: DC sweeps of individual devices to verify behavioral models, simulation of a single dynamic stage to verify functionality, and simulation of multiple stages to evaluate the effects of nanowire cascading, charge sharing and diminished noise margins.

IV. Device Characterization

The xnwFET structure used in our simulations is shown in Fig.3. Rectangular gate and channel silicon nanowires with square cross sections have been considered. The top gate dielectric and bottom insulator are silicon dioxide. In addition, abrupt source-drain junction doping profiles have been assumed.

Unlike the 2D approach commonly adopted in bulk FET analyses, the 3D device simulations are necessary because the assumption of negligible variation along the *y*-direction (as in Fig. 3a) no longer applies to our characterizations of the xnwFET with an unconventional geometry. We have first validated our simulators and simulations against well characterized experimental data on gate-all-around nanowire FETs [17][18]. We have then employed a similar methodology to model both the xnwFET electrostatics and switching operations. Our goal is to design xnwFETs with inversion mode operation, a positive V_{TH}, and $V_{DD} \leq 1$V.

We have performed drift-diffusion simulations on xnwFETs with the parameters listed in Table I. The gate and channel NWs are of the same width for ease of manufacturability. All devices have a relatively high *p*-type doping of 10^{19} cm^{-3} on the channel nanowire to simultaneously suppress short-channel effects and increase V_{TH}. The gate nanowire, source-drain junctions, and substrates are heavily *n*-doped to 10^{20} cm^{-3} to minimize series and contact resistances.

TABLE I. Devices Explored

Device	Gate & Channel NWs	N_{ch}	$N_{G/S/D/Sub}$	V_{Sub}	Underlap
#1	10×10 nm^2	10^{19} cm^{-3}	10^{20} cm^{-3}	0 V	0 nm
#2				0 V	7 nm
#3				-1 V	7 nm

As illustrated in Fig. 3b, Device #1 suffers from very severe short-channel effects in which the off-state current (at V_{GS} = 0V) is very large even with a very high channel doping. In other words, its very poor on-to-off current ratio renders this device useless. To mitigate the xnwFET short-channel effect, we have applied an underlap between the gate edge and source-drain junctions (as illustrated in Fig. 3a) for Device #2. Although a decent on-to-off current ratio could thus be achieved, the device V_{TH} is still slightly off. To satisfy the NASIC requirement, we have additionally applied a negative substrate bias (with respect to the source potential) for Device #3. Finally, we are able to attain a good on-to-off current ratio $\geq 10^3$ and a positive V_{TH} of 0.23 V.

In subsequent sections we will continue to follow the numbering for devices used in Table I for simplicity.

V. Circuit Simulation Results and Validation

DC sweep analysis was done to verify that the models fit closely with Sentaurus device simulation data. The following experiments were then carried out:

A. Validation of Dynamic Circuit Style

The dynamic circuit style presented in Section II was evaluated with the xnwFET devices in HSPICE. V_{DD} for Device #2 was chosen at 0.8 V. V_{DD} for Device #3 was chosen at 1 V. The latter has a positive V_{TH} of around 0.23 V. Therefore, when these *n*-type devices are used for pulling up circuit nodes, the voltage at the node will not reach the full V_{DD} but a value close to (V_{DD} - V_{TH}) [19]. The higher V_{DD} was chosen to provide significant noise margin in the ON-region of the device. Noise and signal degradation issues will be dealt with in more detail in subsequent experiments. Contact resistance to V_{DD} and V_{SS} was chosen to be 10kΩ. Dynamic

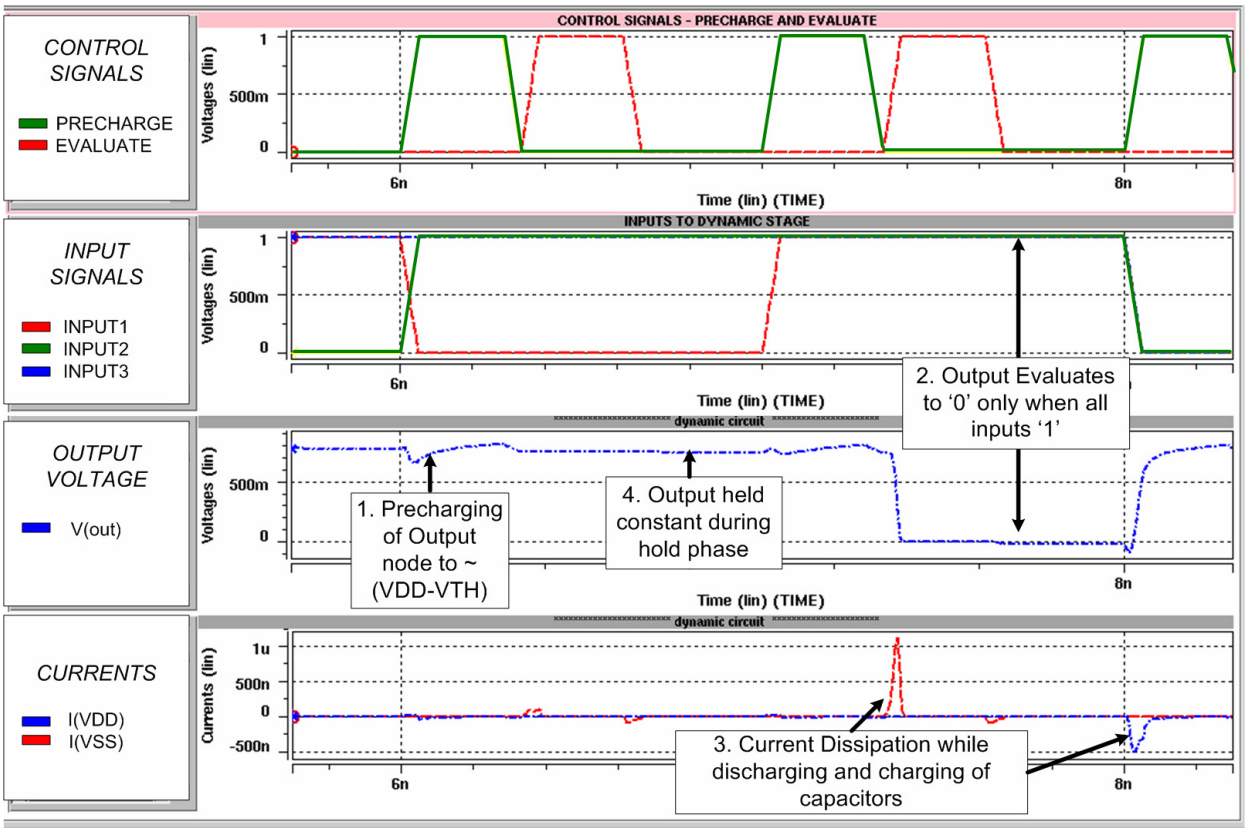

Figure 4. Simulation waveforms for a single NASIC dynamic stage.

control signals operate at a frequency of 1 GHz, with a 33% duty cycle (representing 3-phases - precharge, evaluate, hold - of the dynamic stage).

Fig. 4 shows the functioning of a single NASIC dynamic stage. The top panel shows precharge and evaluate control signals operating at 1 GHz. Panel 2 shows three input signals to the dynamic stage. The output node is shown on panel 3 and the current dissipation shown in panel 4. We make the following key observations from the waveforms (labeled on the diagrams):

1. During precharge, the output node is pulled up to approximately (V_{DD}-V_{TH}), as expected with inversion mode *n*-type devices. By choosing V_{DD} at 1 V for Device #3, we ensure sufficient noise margin for the ON-region operation of the device.

2. During evaluation output goes to GND only when all 3 inputs are at V_{DD}, accomplishing the correct NAND functionality.

3. Charge dissipation occurs only during transitions of control signals corresponding to drawing charge from a source or discharging to ground. There is no static current, implying that at least one of precharge/evaluate transistors is strongly turned off.

4. During hold phase (both precharge and evaluate off) the charge at the output node is almost constant (some minor charge sharing effects exist). As shown in the next section, a constant voltage in the hold phase is very important for cascading multiple dynamic stages.

B. Cascading of Multiple Dynamic Stage

NASIC systems are typically pipelined structures, with multiple dynamic stages cascaded together for implementing logic functionality. In this section we explore these cascaded dynamic structures and seek to validate them for the devices under consideration.

Fig. 5 shows a circuit with 3 dynamic stages used for

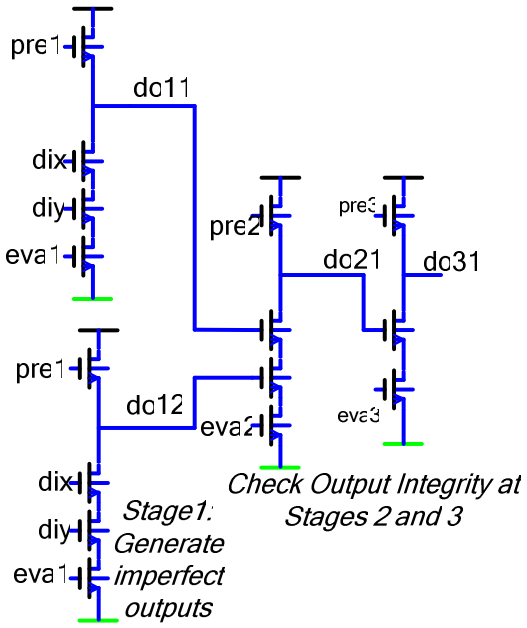

Figure 5. Circuit for validation of cascading in dynamic NASIC design.

evaluating cascading. Stage 1 generates logic '1' signals that may be imperfect (the voltage value can be below V_{DD} due to threshold voltage and charge sharing effects). The output integrity of signals at stage 2 and 3 is checked to ascertain correct propagation. Stage 3 has a single input; this is a 'worst-case' scenario for signal integrity, since it corresponds to the least total effective resistance and capacitance between the output and V_{SS}. A small positive voltage at the input of stage 3 may therefore be sufficient to disrupt circuit behavior.

Fig. 6 shows the circuit characteristics using Device #2 with V_{TH} close to zero. Fig. 7 shows the same results using Device #3 in the circuit. In both diagrams, the top panel shows evaluate and output node of Stage 2 (*eva2* and *do2*), and the bottom panel shows the signals for stage3 (*eva3* and *do3*).

By investigating the waveforms in Fig. 6, we see that: *do31* discharges to logic '0' correctly when *do21* is at logic '1'; fluctuations in the ON-voltage of *do21* do not affect this *do31*. However, functionality issues exist when *do21* is pulled down to logic '0'. We see that when *eva2* is de-asserted (hold phase of Stage 2), a small positive potential builds up at *do2*. This positive potential is due to capacitive coupling with the *do1* node which is being precharged during this time. The small positive potential on *do2* causes the input transistor of Stage 3 to operate in the linear region, leaking charge from *do3* and disrupting functionality.

This behavior can be intuitively explained based on the device characteristics. The small V_{TH} value implies that there is very little margin in the OFF region of the device, hence a small positive potential is sufficient to switch the device on. It

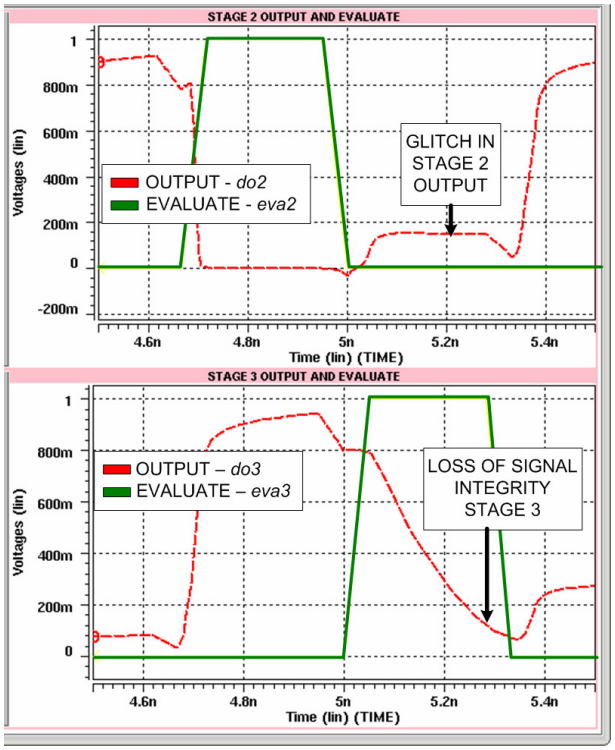

Figure 6. Results from evaluation of cascading using 10/10 devices with no substrate biasing. The small Vth implies that a small glitch at the input is sufficient to turn on the xnwFET leading to errors

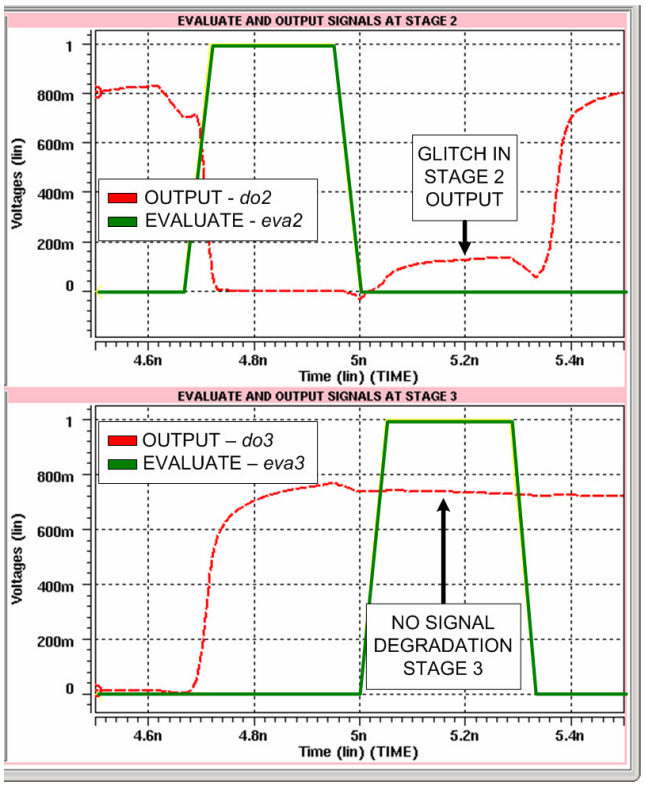

Figure 7. Results from evaluation of cascading using 10/10 devices with substrate bias. Vth=0.23V implies that a glitch at the input does not cause xnwFET to incorrectly switch on.

is expected that by making the V_{TH} higher and providing a larger OFF voltage margin, correct circuit functionality may be achieved.

Applying a -1 V substrate bias with gate underlap of 7 nm can achieve the requisite device behavior by shifting the V_{TH} to +0.23 V. Fig. 7 shows the results for cascading device #3. We see that while the glitch still occurs at *do2*, there is practically no impact on the output node of Stage 3, since the input xnwFET remains in the off region.

C. *Impact on Noise Margin*

N-type devices are used to pull up output nodes, leading to output potentials below V_{DD}, typically around (V_{DD} - V_{TH}) [19]. One important consideration is, will cascading of multiple dynamic stages lead to accumulation of V_{TH} drops, causing incorrect functionality? The NASIC logic style is designed such that this catastrophic noise build-up scenario never occurs.

NASICs use a NAND-NAND logic style which, in addition to being able to implement any arbitrary logic function, is also inverting in nature. We see that while logic '1's are not precharged up to V_{DD}, they always gate a xnwFET in the next stage that is part of a pull down network. In other words, the logic style is such that logic '1' inputs when evaluated will cause logic '0' output at the next stage. Output signals at any stage do not gate xnwFETs in pullup networks; the pull-up is accomplished entirely by precharge signals driven from external CMOS circuitry. Therefore, a combination of circuit

and inverting logic style prevents noise accumulation in NASIC designs. Our experiments have shown that there is no noise accumulation in cascaded dynamic circuits 40 stages deep.

VI. MANUFACTURING IMPLICATIONS

Manufacturing of nanodevice based computational systems continues to be very challenging. Therefore, while devices should possess the requisite characteristics to meet circuit requirements and expected functionality, it is equally important that they can be integrated in a manufacturing process without introducing new challenges. For example, while large gate to channel ratios (e.g. 20×20 nm^2 gate, 10×10 nm^2 channel) can achieve the required electrostatic control and device characteristics including V_{TH} and ON/OFF current ratios, the inherent problem with these is the dissimilar gate and channel dimensions. Since the output node of one nanowire acts as gate for the next stage, using 20/10 devices would need asymmetry along the length of the nanowire. This would require varying the radius during growth of nanowires themselves or contacting nanowires of different diameters together after transferring to a substrate. Nanowires with identical gate and channel dimensions do not have these issues, but may suffer from poor electrostatics as shown in this paper. We therefore tune electrical characteristics using techniques such as underlap and substrate biasing. V_{TH} tuning using these techniques does not impose any new manufacturing challenges. Biasing in NASIC designs is done for the entire circuit, which is much simpler than biasing individual devices. Furthermore, nanowires with rectangular cross-sections and sub-10nm diameter have been shown using the SNAP process [12]; other techniques for growth and alignment are currently being researched. Combined with the circuit evaluations, we believe that these xnwFET devices can be a suitable candidate for realizing future nanoscale fabrics.

VII. CONCLUSIONS

A methodology for integrated device-circuit explorations of nanodevice based systems was presented. This methodology provides a fast and accurate way to create behavioral models for circuit simulations from device data using regression analysis. Furthermore, this approach is very generic, and can be applied to any nanodevice based computing system.

Cascaded crossbar dynamic circuits were validated using this integrated approach that combines circuit simulations, regression analysis, and accurate 3-D physics based device models. Three different xnwFETs were investigated; a xnwFET with 10 nm gate, 10 nm channel, underlap of 7 nm and a substrate bias of -1 V was found to meet circuit requirements including sufficiently high on/off ratios and a V_{TH} of +0.23 V. Circuit simulations show that this device combined with NASIC circuit and logic styles can achieve correct cascading with adequate noise margins. Detailed evaluations of key system level metrics such as power and frequency for large scale designs as well as device/circuit level explorations to achieve optimal system level performance is part of our future work.

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