NASICs: A Nanoscale Fabric for Nanoscale Microprocessors

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***Abstract*- The rapid progress of manufacturing nanoscale devices is pushing researchers to explore appropriate nanoscale computing architectures for high density beyond the physical limitations of conventional lithography. However, manufacturing and layout constraints, as well as high defect/fault rates expected in nanoscale fabrics, could make most device density lost when integrated into computing systems. Therefore, a nanoscale architecture that can deal with those constraints and tolerate defects/faults at expected rates, while still retaining the density advantage, is highly desirable. In this paper, we describe a novel nanoscale architecture based on semiconductor nanowires: NASICs (Nanoscale Application Specific ICs). NASIC is a tile-based fabric built on 2-D nanowire grids and NW FETs. WISP-0 (Wire Streaming Processor) is a processor design built on NASIC fabric where NASIC design principles and optimizations are applied. Built-in fault tolerance techniques are applied on NASICs designs to tolerate defects/faults on-the-fly. Evaluations show that compared with the equivalent CMOS design with 18nm process (the most advanced technology expected in 2018), WISP-0 with combined built-in redundancy could be still 2~3X denser. Its yield would be 98% if the defect rate of transistors is 5%, and 77% for 10% defective transistors.**

I. INTRODUCTION

The scaling trends of MOS devices are expected to reach the fundamental limits in 10 to 20 years. Researchers are looking for alternative device that can go beyond the end of CMOS roadmap. Nanodevices based on semiconductor nanowires (NWs) and carbon nanotubes (CNTs) are perhaps the most promising candidates for high-density computing systems. Several architectures have been proposed based on NWs and CNTs. Examples include [1][2][3][10].

The fabric architecture we proposed is based on semiconductor NWs and targeting microprocessor designs. We call the fabric *NASIC* (Nanoscale Application-Specific Integration Circuits). NASIC is a tile-based fabric on 2-D NW grids. While still based on 2-level logic (e.g., AND-OR logic or equivalents), NASIC designs are optimized towards specific applications for higher density. Sequential circuits and pipelines are implemented with a novel dynamic circuitry in NASIC designs.

With NASIC as underlying fabric, nanoscale microprocessor designs are being explored. For example, the Wire Streaming Processor (WISP-0) is a processor design that exercises many NASIC design principles and optimizations. 5-stage processor pipeline structure is built in 5 dynamic NASIC tiles. In WISP-0, in order to preserve the density advantage of underlying nanodevices, data are streamed through the fabric with minimal control/feedback paths. In this paper, WISP-0 is also used as a prototype design to evaluate various characteristics of NASIC fabric including density, speed, power consumption and fault-tolerance strategies.

Nanodevices have shown great density advantage over MOS devices. Integrating them into a real computing system is, however, facing many challenges. One of the key aspects for nanoscale computing systems is reliability. Researchers have pointed out that the defect rate at device level is expected to be a few percent [5], much higher than conventional MOS devices. Traditional fault tolerance/detect techniques in CMOS are not suitable for nanoscale systems because they assume very low defect rates and arbitrary routing of wires. We need new fault tolerance strategies designed for nanofabrics to keep the system functional when a substantial part of system is faulty.

Basically there are two main approaches proposed to handle faults at nanoscale. First, if reconfigurable devices are available, we may be able to reconfigure around defective devices after manufacturing. This approach, however, has many challenges: 1).A complex nano-micro interface is required to access every nanodevice for reconfiguration purpose. 2). An accurate defect map for nanoscale circuits has to be extracted through a limited number pins. 3). Reconfiguration-based approaches would primarily address permanent defects. It might be difficult to mask faults due to transient errors or processor variation.

Alternatively, as proposed in this paper, we can introduce built-in redundancy to automatically mask faulty signals. Compared with reconfiguration approaches, this strategy might also mask transient faults from external noises or crosstalk. The accessibility to any single nanodevice is not necessary for this approach. This fact significantly simplifies the nano-micro interfacing. Furthermore, defect maps are not needed anymore. These aspects provide the computing systems relying on built-in redundancy, e.g. WISP-0, great advantages.

We develop simulation tools to evaluate the power consumption, density, and the yield of NASIC designs. Evaluations show that compared with the equivalent CMOS design with 18nm process (the most advanced technology expected by ITRS in 2018 [19]), WISP-0 with error-correcting circuitry could be 7~9X denser. The yield of WISP-0 is 60% if 5% of transistors are defective, and 10% for

10% defective transistors. After combined with system-level CMOS voting, the density would still be 2-3X denser and the yield could be as high as 98% for 5% defect rate and 77% for 10%. Preliminary estimations indicate that NASIC designs are significantly faster than CMOS and the power consumption trends are orders of magnitude lower than those in conventional CMOS technologies.

The rest of paper is organized as follows: Section II provides an overview of NASIC circuits and WISP-0. Built-in fault-tolerance techniques for NASICs are also discussed in this section. The yield and density evaluations for WISP-0 are provided in Section III. Speed and power consumption are discussed in Section IV. Section V concludes the paper.

II. NANOCIRCUITS, NASICS AND WISP-0 PROCESSOR

A. *Dynamic Nanocircuits on Semiconductor Nanowires*

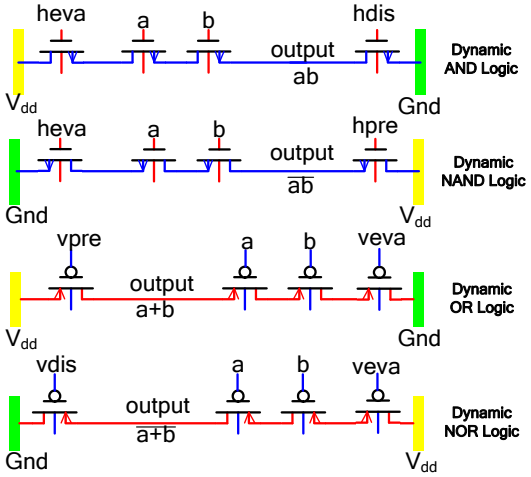

Fig. 1. Dynamic circuits implementing AND, NAND, OR and NOR logic functions on NWs.

Dynamic circuits have been widely used in MOS-based systems. We can similarly implement dynamic circuits at nanoscale with the help of control signals generated in CMOS. For example, Fig. 1 shows how to implement basic logic functions (i.e., AND, NAND, OR and NOR) in a dynamic style on semiconductor NWs.

A novel aspect of dynamic circuits in NASICs is the addition of a *hold* phase that is used to enable correct cascading. A variety of schemes have been proposed achieving different throughputs. In NASICs, this *hold* phase also provides temporary storage of output values on NWs. Details regarding this aspect could be found in [6][7].

A. *Overview of NASICs*

NASIC designs are based on dynamic circuits implemented on semiconductor NWs; various optimizations are applied to work around layout and manufacturing constraints as well as defects [8][9]. While still based on cascaded 2-level logic style, e.g., AND-OR, NASIC designs are optimized according to specific applications to achieve higher density and defect/fault-masking. The selection of this logic family is due to its simplicity and applicability on a 2-D style fabric where arbitrary placement and routing is not possible. Furthermore, due to manufacturing constraints (such as layout and uniform doping in each NW dimension) it may be impossible to use, for example, complementary devices close to each other, such as in CMOS or orient devices in arbitrary ways. By using dynamic circuits and pipelining on the wires, NASICs eliminate the need for explicit flip-flops in many areas of the design [6] and achieve unique pipelining schemes.

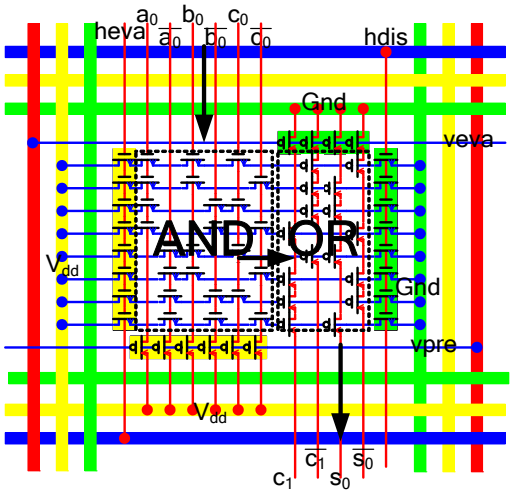

Fig. 2. 1-bit dynamic NASIC full adder using AND-OR cascaded logic. Arrows show propagation of data through the tile.

Fig. 2 demonstrates the design of a simple 1-bit NASIC full adder in dynamic AND-OR style [7]. The thinner wires represent NWs. All horizontal NWs are doped to n-type while all vertical NWs are doped to p-type. The control signals *hdis*, *heva*, *vpre*, and *veva*, correspond to discharge, evaluation, precharge and evaluation operations on different NWs. Each nanotile is surrounded by microwires (MWs) (thicker wires in the figure), which carry ground (*Gnd*), power supply voltage (V_{dd}), and control signals for the dynamic evaluation of outputs. The control signals are generated in CMOS. As we mentioned before, complementary signals are required to implement arbitrary logic functions in 2-level logic style. In the circuit in Fig. 2, we generate negative outputs $\sim c_1$ and $\sim s_0$ for cascading in multi-tile designs. Please refer to [6][7][8][9][10] for more details.

NASIC manufacturing may be accomplished through a combination of self-assembly and top-down processes.

- NWs can be grown using seed catalyst techniques or other methods that may ensure uniform NW diameters [11]. NWs may be aligned into parallel sets using Langmuir-Blodgett techniques or nanopatterning.
- Regions on individual NWs where there should be no FET channels will then need to be metallized using a lithographic mask. A 2NW pitch resolution is required but precise shaping is not needed, making this step easier than a CMOS manufacturing step for a comparable feature size.
- An oxide layer may then be grown over the NWs and a 2D grid formed by moving one NW set on top of the other.
- A fine grain metallization step demarcates FET channels,

create metallic interconnect between neighboring FETs. This may be achieved by using the top NW as a self-aligning mask as shown in [12].

- Micro-nano interfacing can be done in conjunction with lithographic process steps.

B. Single-Type vs. Complementary Type NASICs

In order to produce complementary FETs, two different types of doped NWs must be used. Complementary FETs have been demonstrated in zinc oxide [13], silicon [11], and germanium [14], but in all cases differences in transport properties were found between the two types, sometimes much greater than those seen in today's traditional CMOS FETs. By suitably modifying the NASIC dynamic control scheme and circuit style, we can implement arbitrary logic functions with one type of FETs in NASICs. A design using only n-type FETs (nFETs) will implement a NAND-NAND cascaded scheme whereas a design using only p-type FETs (pFETs) will implement a NOR-NOR scheme. Fundamentally, these are equivalent with the original AND-OR. These schemes may thus be used with manufacturing processes where complementary devices are difficult to achieve. The 1-bit adder example with nFETs is shown in Fig. 3. A detailed analysis of the control scheme for this circuit is beyond the scope of this paper.

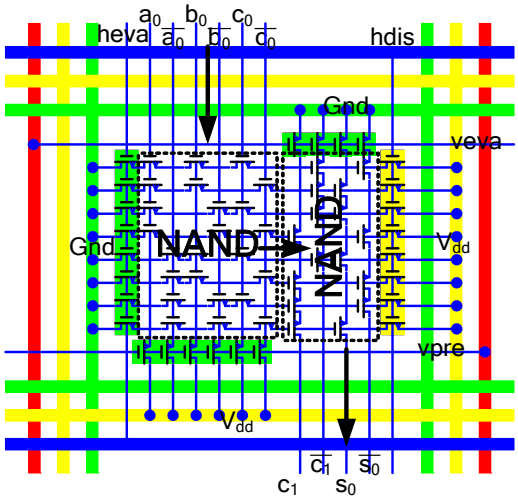

Fig. 3. nFET only version of a 1-bit adder using the NAND-NAND cascaded logic.

C. Combine Logic Families in NASIC Fabric

Comparing dynamic AND and NAND circuits, we find that the only difference between them is their connections to V_{dd} and *Gnd*. Complementary outputs can be easily generated by interchanging the power and ground NWs. Similar observation can be made for dynamic OR and NOR circuits. For the design in Fig. 2, if an original output is generated with OR circuits and its complementary version is generated with NOR circuits, they would share the same horizontal NWs as partial products. This way we may reduce the number of horizontal NWs and indirectly reduce the associated transistors on these NWs.

Fig. 4 shows the design of the same 1-bit adder combining OR and NOR circuits in the same plane. Note that the top horizontal NW in Fig. 2 is now unnecessary and therefore removed from the design in Fig. 4. A key advantage of this new fabric is that it effectively improves the density but does not introduce new manufacturing requirements. The only modification required is the connections from NWs to V_{dd} and *Gnd* MWs. This can be made in a fashion similar to the original process. The dynamic control scheme otherwise remains completely unchanged. This hybrid logic technique may also be suitable to other 2-level logic families. For example, on nFET-only NASIC fabrics, we can combine NAND-NAND and NAND-AND logic families to achieve the same optimizations. For NOR-NOR based CMOL fabric [5], NOR-NOR and NOR-OR can be combined.

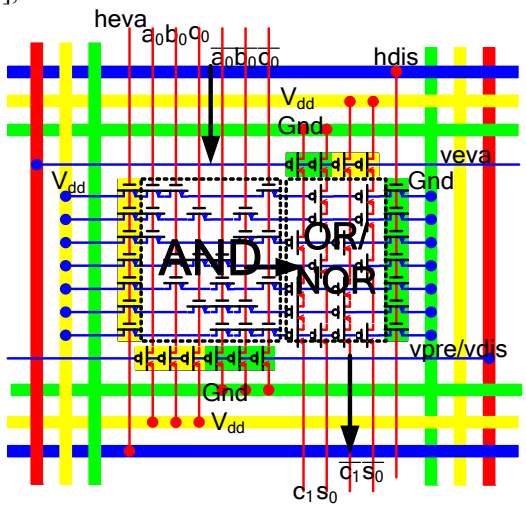

Fig. 4. A 1-bit adder using the AND-OR/NOR logic.

Another interesting benefit of the hybrid AND-OR/NOR fabric is that it also improves the yield of NASIC designs. The reason is quite simple: The total number of horizontal NWs and associated transistors are reduced compared to the original design. For a given defect rate, the expected number of defects in a design is also reduced. A design can therefore achieve better yield in hybrid AND-OR/NOR fabric as compared to the original AND-OR.

D. Overview of the WISP-0 Processor

WISP-0 is a stream processor that implements a 5-stage pipelined streaming architecture in 5 NASIC tiles: *PC*, *ROM*, *DEC*, *RF* and *ALU*. Local communication between adjacent nanotiles is provided by NWs. Each tile is surrounded by MWs which carry ground, power supply, and some control signals. WISP-0 uses a 3-bit opcode and 2-bit operands. It supports many different arithmetic operations including multiplication.

Fig. 5 shows the layout of WISP-0 with AND-OR logic style. A NASIC tile is shown as a box surrounded by dashed lines. More details about the various circuits used can be found in [6][7][9]. In this paper, we use WISP-0 mainly to evaluate our new nanofabric and focus on the density and fault-tolerance related tradeoffs and implications.

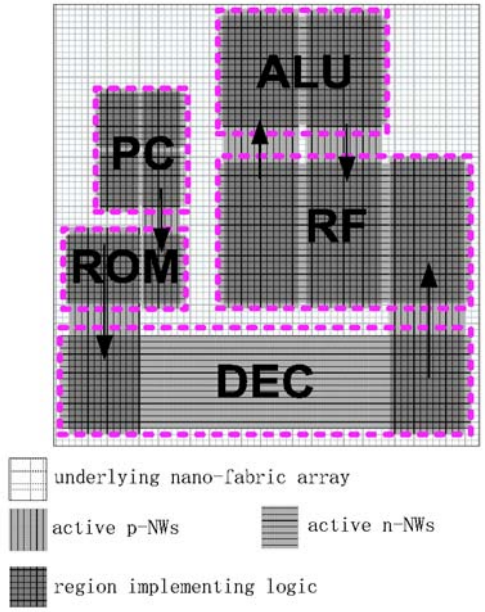

Fig. 5. Floorplan of the WISP-0 processor.

E. *Built-in Fault-tolerance in NASICs*

Nanoscale computing systems including NASICs have to deal with the high defect rates of nanodevices and faults introduced by manufacturing of fabrics. In NASICs we consider a fairly generic fault model with both uniform and clustered defects and three main types of permanent defects: NWs may be broken, the transistors at the crosspoints may be stuck-on (no active transistor at crosspoint) or stuck-off (channel is switched off).

We consider defect rates of up to 15% at the finest granularity which is the device level. Our previous work indicates that device-level defect rates greater than 15% would likely eliminate the density benefits of nanoscale fabrics compared to projected CMOS technology, in the context of microprocessor designs. We also assume that the stuck-on transistor is much more prevalent than stuck-off in NASIC fabric due to the metallization process [15] in manufacturing steps. Stuck-off transistors can be treated as broken NWs.

Built-in fault-tolerance techniques are applied at various granularities for NASICs to make NASIC designs functional even in the presence of errors, while carefully managing area tradeoffs. The built-in fault-tolerance techniques that are applied on NASIC fabric include 2-way redundancy, error-correcting circuitry and system-level voting (i.e., TMR) in CMOS at key architectural points. Comprehensive description of built-in fault-tolerance techniques in NASICs can be found in [10][17] and is beyond the scope of this paper. The density and yield of WISP-0 under different fault-tolerance scenarios are evaluated and presented in the next section.

III. Yield and Density Evaluations

We can incorporate a variety of fault-tolerance techniques into all circuits of WISP-0 [7]. To verify the efficiency of our fault-tolerance approaches, we developed a simulator to estimate the yield of WISP-0 for different defect rates and also considered other error sources.

A. *Yield Evaluation of WISP-0*

The simulation results for permanent defects are provided in Fig. 6 (assumes stuck-on FETs) and Fig. 7 (assumes broken NWs). We assume defects are uniformly distributed.

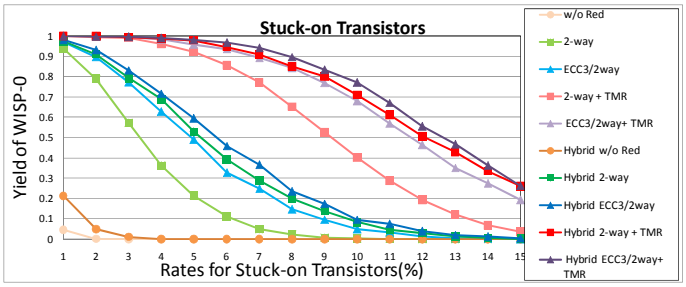

Fig. 6. The yield achieved for WISP-0 with different techniques when only considering stuck-on transistors.

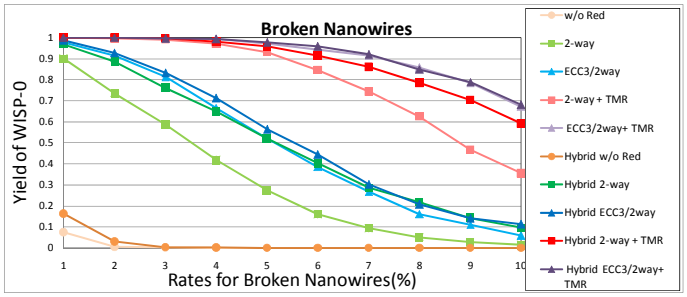

Fig. 7. The yield achieved for WISP-0 with different techniques when only considering broken NWs.

The notation used is: *w/o Red* stands for WISP-0 without redundancy; *2-way* stands for WISP-0 with 2-way redundancy; *2-way+TMR* stands for 2-way redundancy plus micro-scale; *ECC3/2way* denotes a design with error-correcting circuits with Hamming distance of 3 on vertical NWs and 2-way redundancy on horizontal NWs; Prefix *Hybrid* stands for the hybrid AND-OR/NOR logic. While other combinations are possible, we found these to be most insightful and representative.

From the results, we can see that our built-in fault-tolerance techniques work very well for defective transistors and broken NWs. Without built-in redundancy, the yield of WISP-0 goes down to 0 when defect rate are 3%. The yield of WISP-0 with 2-way redundancy is still over 20% when 5% transistors are defective. With error-correcting technique, we may achieve the yield of WISP-0 as high as 48% for the same defect rate. Hybrid logic improves the yield of WISP-0 significantly, especially for 2-way redundancy technique. The improvement is 15% for 2% defective transistors and 2.5X for 5%. For WISP-0 with ECC3/2-way, the yield improvement of hybrid logic is 21% for 5% defective transistors. Similar observations can be achieved for broken NWs.

The built-in fault-tolerance techniques proposed in this paper can deal with more than permanent defects. Transient faults (i.e., soft errors) due to external noises or crosstalk can be masked as well. We refer readers interested in this aspect to [10].

B. *Density Comparison with Equivalent CMOS Processor*

The normalized density of WISP-0 for the various scenarios is shown in Fig. 8. We assume that NW pitch is 10nm and MW pitch is 42nm at 18nm CMOS technology node according to ITRS prediction [19]. To get a better sense of what the densities actually mean we calculate the density of an equivalent WISP-0 processor: we designed this processor in Verilog-HDL, synthesized it to 180nm CMOS. We derived the area with the help of the Synopsys Design Compiler tool. Next, we scaled it to projected 18nm technology node, assuming area scales down quadratically. For the purpose of this paper, we assume that the CMOS version of WISP-0 is defect-free and no fault-tolerance technique is applied.

We can see from the results that the area overhead of adding 2-way redundancy for the nanoscale designs is roughly 3X when MWs in NASICs are assumed to have the same dimensions as metal wires (Layer 1) in 18nm CMOS technology. TMR-related overhead added to the nanoscale design brings an extra 3X overhead because TMR requires 3 copies of nanoscale blocks. A WISP-0 design based on *ECC3/2-way* requires around 40% more area than one based on 2-way redundancy for both horizontal and vertical NWs, but achieves a better yield.

Overall, the density of a NASIC-based WISP-0 (AND-OR logic) remains at least 2X (with ECC3/2-way and TMR) or 7X (with ECC3/2-way only) greater than the density of the corresponding CMOS processor at 18nm. Hybrid AND-OR/NOR logic improves the density of WISP-0 significantly. The density improvement is 50% for 2-way version and 29% for ECC3/2-way.

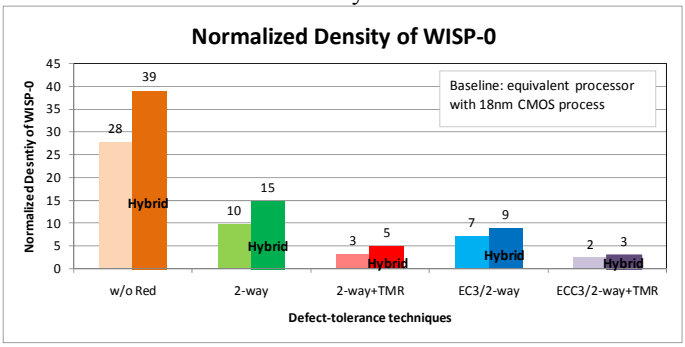

Fig. 8. Normalized WISP-0 density with different defect tolerance techniques.

IV. Speed and Power Estimations

Delay and power estimation was done for the WISP-0 processor built on silicon nanowires.

A NW-MW contact resistance of 10kΩ and resistivity values of 10^{-7}Ω-m and 10^{-5}Ω-m for NiSi and Si respectively were used in these calculations [18]. R_{ON} for a transistor of length 5nm and width 4nm was calculated to be around 4kΩ. An R_{OFF} resistance of 10GΩ was used [1]. A nanowire pitch of 10nm, an oxide layer thickness of 1nm, and a dielectric constant of 2.2 were assumed. Table I summarizes all the parameter values used in these calculations.

TABLE I
PARAMETER VALUES

NW-pitch	10nm
NW-shell thickness (t_{sh})	1nm
NW-width (w)	4nm
Dielectric Constant of SiO_2(ε_r)	2.2
Resistivity of Si (ρ_{Si})	10^{-5} Ωm
Resistivity of NiSi (ρ_{NiSi})	10^{-7} Ωm
NW-MW contact Resistance (R_c)	10 kΩ
Transistor ON Resistance (R_{ON})	4 kΩ
Transistor OFF Resistance(R_{OFF})	10 GΩ
Supply Voltage	3V-4.5V

A. *Delay Calculations*

A lumped RC model was used for the worst-case delay analysis. Expressions from [1] were used for capacitance estimation. These calculations take into account NW-NW junction capacitances and relatively realistic coupling scenarios. The coupling capacitance per unit length was found to be 39.04pF/m. The junction capacitance was found to be 0.652aF.

TABLE II
CAPACITIVE LOADING (aF)

	Control NW(H)	Datapath NW(H)		Control NW(V)	Datapath NW(V)	
	pre/eva	pre	eva	pre/eva	pre	eva
PC	14.99	9.78	25.27	11.08	4.56	32.43
ROM	8.48	11.08	33.47	9.78	20.12	82.68
DEC	11.74	20.21	83.33	11.74	55.42	143.1
RF	27.38	26.73	98.21	9.13	42.38	167.6
ALU	29.34	18.26	37.78	16.95	30.64	138.7

Table II indicates the capacitive loading on each tile of WISP-0 for different clock phases. During each phase, there is one control NW and one or more datapath NWs switching. In the table 'Control NW (H)' refers to a horizontal precharge/evaluate signal. Since the precharge and evaluate control NWs in one plane are geometrically identical, the capacitive loading on these NWs is the same. 'Datapath NW (V)' refers to datapath nanowires in the vertical plane. The capacitive loading during precharge and evaluate is dissimilar for datapaths owing to different lengths and coupling effects.

The lumped capacitance is in the range of ado-Farads, and as expected, larger components such as the RF (Register File) are more heavily loaded. Table III shows the maximum delay for the tiles of WISP-0 assuming a MW-NW contact resistance of 10kΩ. 'H-pre' and 'V-pre' stand for horizontal precharge and vertical precharge phases respectively, 'H-eva' and 'V-eva' are horizontal and vertical evaluate phases. All delays are in picoseconds.

TABLE III
DELAY (ps)

	H-pre	H-eva	V-pre	V-eva
PC	0.227	0.463	0.141	0.536
ROM	0.215	0.796	0.302	3.785
DEC	0.375	1.485	0.934	2.742
RF	0.596	2.135	0.615	4.778
ALU	0.481	1.415	0.667	3.667

In WISP-0, datapath lengths and the number of transistors on each datapath are different. Consequently the delay varies over a wide range of values. However, the performance of a pipeline is determined by the slowest segment; in this case it is the vertical

plane of the RF (delay=4.778ps). The operating frequency assuming a 33% duty cycle (reflecting a clock needed for a precharge-evaluate-hold control) is easily shown to be 69GHz. It is expected that the frequency will be lower in practical designs with longer datapaths and larger bitwidths.

The contact resistance of 10kΩ is a large contributor to the overall delay for all nanotiles. With improvements of manufacturing, this value is expected to be significantly reduced.

B. Power Estimation

The average dynamic power and the leakage power were estimated for the tiles of WISP-0. Dynamic power calculations were done for a 69GHz operating frequency for a range of typical operating voltages between 3V-4.5V – the voltage is estimated based on the original NW FET papers. The expression used is:

$$P_{dyn} = \sum_{pre,eva} (C_{L1} + N * C_{L2}) * V_{DD}^{2} * f$$

Where f is the operating frequency, C_{L1} is the capacitance on the control nanowire and C_{L2} is the capacitance on a datapath nanowire. N is the number of datapath nanowires switching simultaneously. In cases where N is variable (e.g., application specific), an average value is chosen assuming a 50% switching probability.

TABLE IV
DYNAMIC POWER CONSUMPTION (μW)

	3V	3.5V	4V	4.5V
PC	213	290	380	481
ROM	377	509	665	841
DEC	977	1330	1738	2199
RF	2780	3784	4942	6254
ALU	447	609	795	1007

Table IV shows the dynamic power consumption (in μW) for the components of WISP-0 at the 69GHz frequency. It is seen that the Register File consumes maximum average dynamic power. This is due to a large capacitive load owing to the relatively large size of the tile. The power consumption trends on the whole are orders of magnitude lower than those seen in conventional CMOS technologies.

Leakage power consumption of NASIC tiles is negligibly small (in the order of nano-Watts) because R_{OFF} resistance is around 10GΩ [1].

V. CONCLUSIONS

In this paper we provided a comprehensive overview of a nanoscale fabric called NASIC for computing systems. We showed how to build a nanoscale microprocessor on 2-D NASIC fabric. A new dynamic circuit design was proposed for efficient cascading and pipelining. With built-in fault-tolerance techniques, we can tolerate faults from a variety of sources and still achieve considerably higher density than in an equivalent CMOS design at the end of the projected ITRS roadmap. NASIC-based processors show great promise due to the combination of fault-masking, high density, and scalability.

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