

CMOS Control Enabled Single-Type FET NASIC

Pritish Narayanan, Michael Leuchtenburg, Teng Wang, Csaba Andras Moritz
University of Massachusetts, Amherst MA 01003 USA
{pnarayan,andras}@ecs.umass.edu

Abstract

A new hybrid CMOS-nanoscale circuit style has been developed that uses only one type of Field Effect Transistor (FET) in the logic portions of a design. This is enabled by CMOS providing control signals that coordinate the operation of the logic implemented in the nanoscale. In this paper, the new circuit style is explored, examples from a microprocessor design are shown, performance, manufacturing and density implications discussed. The system is based on the existing CMOS-nano hybrid fabric architecture NASIC, but the new circuit style reduces the requirements on devices and manufacturing from previous NASIC designs, significantly improves performance without any deterioration in circuit density.

1. Introduction

Semiconductor nanowires (NWs) are a promising nanodevice technology, but there are some major challenges to overcome before systems built out of these devices can become a reality. The primary issue is the manufacturability of architectures. It is difficult to reliably construct NW-based systems with good performance characteristics due to both device and manufacturing concerns. Therefore one objective of nanoscale fabric architectures is to minimize underlying manufacturing/ device requirements.

For instance, in designs based on semiconductor NWs, it is difficult to build both p- and n-FETs using the same material. While complementary FETs have been demonstrated in zinc oxide [12], silicon [7], and germanium [10] NWs, in all cases large differences in transport properties were found between the two types of FETs, sometimes much greater than those seen in today's traditional CMOS transistors. As transistor characteristics are certain not to be symmetric between

n-FETs and p-FETs, this would make timing closure complicated thereby making it harder to manufacture systems reliably. Consequently, it would be advantageous if only one type of device were required.

However, conventional logic systems designed using mostly one type of FETs, such as pseudo-NMOS, suffer from power and performance issues as compared to CMOS [14]. This is one reason why these have not found widespread applicability.

By using a fabric style that combines CMOS support with nanoscale logic implementation, these problems can be eliminated. First, instead of using a design style such as pseudo-NMOS, the control scheme may be moved into CMOS and the design modified such that the associated nanoscale circuits could function with only one type of FET. Also, a dynamic scheme may be adopted for the nanoscale logic to minimize leakage power by eliminating direct paths between ground and power rails.

In techniques presented in this paper, a dynamic NMOS style is shown with clock signals generated in CMOS. The new design style is demonstrated with circuit examples and a streaming processor design. It does not incur any density penalty compared to similar design styles using complementary devices and improves circuit speeds by close to 2X. Similarly, a PMOS logic scheme could also be developed. A PMOS version would have the same density but inferior performance compared to the NMOS design.

The rest of the paper is organized as follows. An overview of the NASICs fabric architecture is presented in Section 2 and the new design style is discussed in Section 3. Single-type FET implementation of WISP-0, a NASIC processor, is shown in Section 4. Section 5 contains analysis and evaluation of systems using the single-type FET scheme. Conclusions are presented in Section 6.

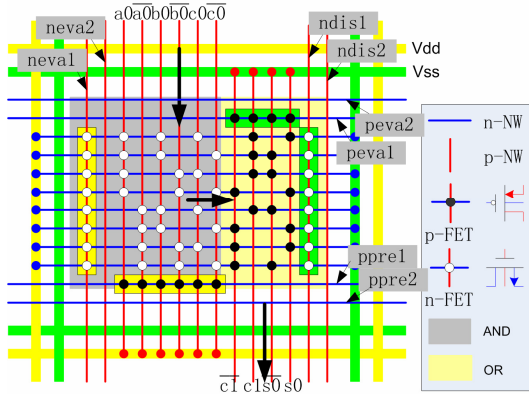


Figure 1. AND-OR implementation of a 1-bit full adder in NASIC.

2. Overview of NASIC

It is possible, with self-assembly techniques, to produce arrays of doped nanowires (NWs) with nanometer pitches. These can then be placed at right angles with each other, forming a grid [8][9]. FETs can be formed at the crosspoints.

NASIC (Nanoscale Application Specific Integrated Circuit) is a fabric architecture based on these sorts of semiconductor NW grids with FETs at crosspoints [1][2][4][5]. NWs are connected to microwires which provide control signals generated from CMOS. The NW grids are laid out in tiles, with each tile implementing two-stage logic with a dynamic control style that channels the flow of data through these tiles.

Previous NASIC implementations have been based on a 2-level AND-OR logic style, involving both n- and p-type FETs. These designs are self-healing: defects are masked using built-in redundancy and error correcting circuits on the nanogrid coupled with system level voting in CMOS. Defect and fault-tolerance are especially important in nano-fabrics where reconfiguration tends to be difficult due to complex nano-micro interfacing required and defect rates will likely be very high. Fault tolerance techniques for NASICs are discussed in [1][2].

In order to provide the reader with an insight into the NASIC fabric architecture, following is a description of the functioning of a NASIC tile.

Fig. 1 illustrates the design of a 1-bit NASIC full adder in a dynamic style with two types of FETs required for AND-OR logic implementation. Each nanotile is surrounded by microwires, which carry V_{dd} and V_{ss} . The control signals *ndis1*, *ndis2*, *neva1*, *neva2*, *ppre1*, *ppre2*, *peva1* and *peva2* represent NWs connected to control microwires. Lines suffixed with '2' are control signals for adjacent tiles. These need to be coordinated with this tile to meet hold-time

constraints. *dis* and *pre* lines are for predischarge and precharge, *eva* lines trigger evaluation.

This tile implements AND-OR logic; The left portion selectively ANDs the inputs, depending on whether a transistor is present for that input on each row, and generates midterms. The right side implements OR logic on these midterms to form the final outputs for the tile. The tile can thus be said to be divided into AND and OR planes.

The inputs flow in from the top, and the outputs flow out from the bottom, on the labeled wires. In NASIC designs, NWs are used to provide communication between adjacent tiles.

Dataflow in NASICs is through a 3-phase progression. The CMOS control signals coordinate these phases.

Phase1: *ndis1* (predischarge n-type NWs) is switched on. This gates the right side of all horizontal NWs to V_{ss} .

Phase2: *ndis1* is switched off and the AND logic plane is evaluated by turning on *neva1*. For example, if the inputs are '111', the horizontal NW gated by *a0*, *b0* and *c0* is pulled to V_{dd} . All other NWs retain logic '0'. Simultaneously, the OR plane, consisting of vertical output p-type NWs running out of the bottom of the tile is precharged to V_{dd} .

Phase 3: *ndis1* and *neva1* signals are switched off, and values evaluated on the horizontal NW in the previous phase are held. These horizontal NWs gate the transistors on the OR plane. The OR Plane consisting of p-type NWs is evaluated (*peva1* transistors are ON) and the outputs generated. The OR plane must now hold its output for an additional phase, having neither *ppre1* nor *peva1* turned on, so that the next tile can use this output as its input. The control of each adjacent tile is hence offset in time from the previous one. Thus, the synchronous switching of control signals generated from CMOS coordinates the evaluation and flow of data through multiple logic tiles in a NASIC fabric.

3. NASICs with single type FETs

3.1. Modifications to the control scheme

It has been found that altering the CMOS control scheme obviates the need for two types of devices to implement arbitrary logic functions on the nanogrid. The scheme may thus be used with manufacturing processes where complementary devices are difficult or impossible to achieve. A design using only n-type FETs will implement NAND-NAND logic. A design using p-type FETs will implement NOR-NOR logic. Fundamentally, these are equivalent with AND-OR.

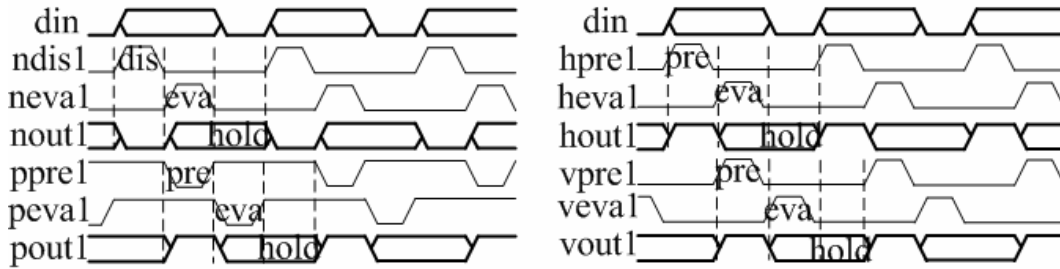


Figure 2. Timing diagrams for Dynamic Control (left) AND-OR with complementary FETs and (right) NAND-NAND with n-type FET

Fig. 2 compares the timing diagrams of cascaded AND-OR (original) and NAND-NAND (proposed) schemes for a nanotile. The control signals for the latter are horizontal and vertical precharge (*hpre1* and *vpre1*) as well as evaluate signals (*heval1* and *veval1*). The ‘n’ and ‘p’ prefixes have been removed since only one type of NW is used. The dynamic 3-phase scheme of precharge, evaluate and hold is still in place. However the behaviour of the control signals has been modified. There is no predischarge phase; all planes are precharged since successive planes implement NAND logic function. Also, all control signals are active high, since they gate only n-type FETs.

3.2 Implementation with n-type devices

Fig. 3 shows a 1-bit full adder built using only n-type devices. Its function is very similar to the circuit with complementary devices. The connections to V_{dd} and V_{ss} have been changed relative to the previous design (Fig. 1) for the horizontal plane.

In comparison with the previous implementation it may be noted that the relative positions of the transistors in the NAND-NAND example is identical to

the AND-OR implementation. The only change from AND to NAND is in the swapping of the control signals, V_{dd} and V_{ss} . The output node is precharged rather than predischarged which results in the inversion of the function. On the second plane, the change is more significant: from OR to NAND. Both the type of the transistor and polarity of the control scheme have been changed. Also, the inputs to the vertical NW are now inverted from their values in the AND-OR scheme. The inversion of the inputs in conjunction with the change from OR to NAND results in a transformation of the logic function. DeMorgan’s Laws tell us that this transformation should produce the same result as the AND-OR scheme. This allows us to maintain the transistors in their original positions, even though the logic functions used have changed. It can thus easily be seen that there will be no impact on the area of the nanotile itself. In addition, the new scheme reduces the number of microwires by using the same function and consequently the same polarity for multiple control signals, thus allowing them to share some microwires.

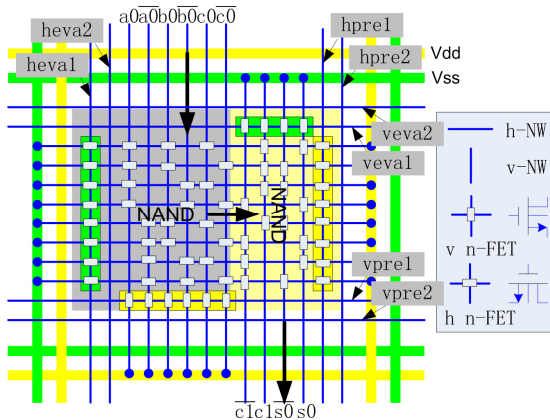


Figure 3. NAND-NAND implementation of a 1-bit full adder in NASIC.

4. Single-type FET implementation of WISP-0

WISP-0 is a stream processor that implements a 5-stage microprocessor pipeline architecture including *fetch*, *decode*, *register file*, *execute* and *write back* stages [4]. Fig. 4 shows its floorplan. A nanotile is shown as a box surrounded by dashed lines in the figure. In WISP designs, in order to preserve the density advantages of nanodevices, data is streamed through the fabric with minimal control/feedback paths. WISP uses dynamic circuits and pipelining on wires to eliminate the need for explicit flip-flops and therefore improve density considerably. All WISP-0 tiles have been implemented using the new control scheme. This section shows two examples.

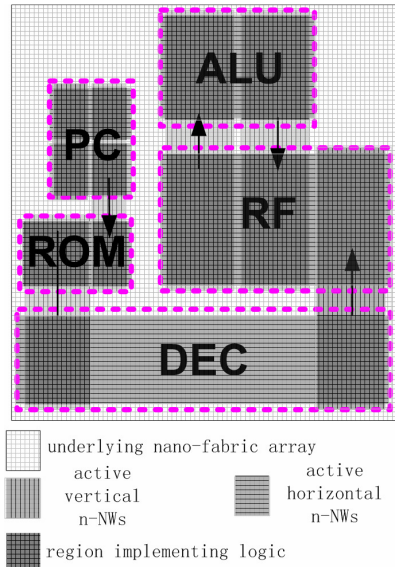


Figure 4. WISP-0 Floorplan

4.1 WISP-0 Program counter

The WISP-0 program counter is implemented as a four bit accumulator. Its output is a four bit address that acts as input to the ROM. The address is incremented each cycle and fed back using a nano-latch. Fig. 5 shows implementation of the Program Counter using NAND-NAND. Diagonal FETs on upper NAND planes delay output by one cycle and allow signals to ‘turn the corner’ [3].

4.2 WISP-0 Arithmetic Logic Unit

Fig. 6 shows the layout of the WISP-0 ALU that implements both addition and multiplication functions. The arithmetic unit integrates an adder and multiplier together to save area. It takes the inputs (at the bottom) from the register file and produces the write-back result. At the same time, the write-back address is decoded by the 2-4 decoder on the top and transmitted to the register file along with the result. The result is written to the corresponding register in the next cycle.

5. Discussion

5.1 Density Evaluation

As shown in the logic diagrams, the NW portion of the area will not change at all, as the transistors are laid out in exactly the same way as in the circuits with two types of transistors. A useful by-product of using a single-type of FET though is a reduction in the number of microwires due to the modifications to the control scheme that allows sharing of some CMOS signals. Reduction in the number of microwires is a density

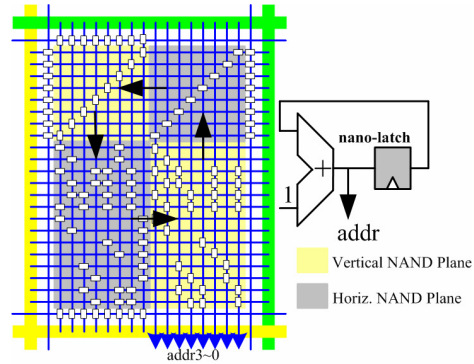


Figure 5. WISP-0 PC with n-FETs

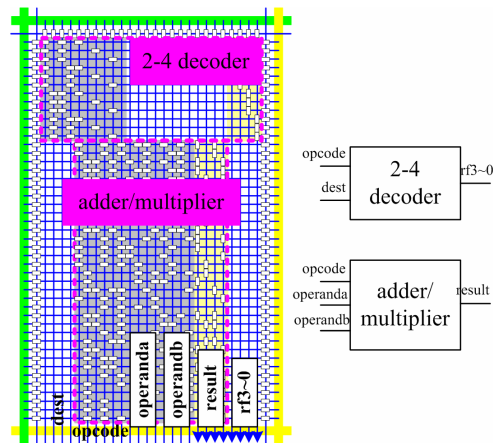


Figure 6. WISP-0 ALU with n-FETs.

advantage, since microwires have tangible area overhead, even at end-of-roadmap feature sizes. The actual benefit would depend on the size of the design – larger designs, where the microwire area is small in comparison to the logic portions, will benefit less. For more information about relative densities of NASICs with various defect-tolerance techniques, please see [1][2][5].

5.2 Performance Evaluation

With schemes such as AND-OR, the performance of the circuit will be limited by the cascaded planes employing the slower devices. Also, since arbitrary sizing of devices on the nanogrid is not achievable, it is not possible to match the performance characteristics of dissimilar devices. Therefore elimination of the slower devices using the new control scheme carries significant performance benefits, despite the fact that the transistors are laid out in exactly the same fashion.

Delay estimation has been done for the tiles of WISP-0 for both the AND-OR and NAND-NAND

logic implementations. A NW pitch of 10nm, an oxide layer thickness of 1nm, and a dielectric constant of 2.2 were assumed. The p-type devices for this evaluation are Silicon NWs (SiNW) lightly doped with Boron. The n-type devices are SiNW lightly doped with Phosphorous. Nanowire transistor length is 5nm and width is 4nm. The ON resistance for these geometries for the two types of devices (R_{ON-P} and R_{ON-N}) has been calculated to be 7.875 k Ω and 3.75 k Ω respectively based on data reported in [6]. Interconnect is created using a Nickel based metallization process, and the resistivity of the NiSi thus formed is assumed to be 10^{-7} Ω -m [11]. The contact resistance is ignored in order to assess the true performance impact of migrating to the single-FET scheme. Table I summarizes all parameter values.

A lumped RC model is used for the worst-case delay analysis. Expressions from [3] were used for capacitance estimation. These calculations take into account NW-NW junction capacitances and relatively realistic coupling scenarios. The coupling capacitance per unit length was found to be 39.04pF/m. The junction capacitance was found to be 0.652aF.

Table II shows the maximum delay for the tiles of WISP-0 for the AND-OR scheme. ‘*ndis*’ and ‘*ppre*’ stand for the n- device discharge and p-device precharge phases respectively, ‘*neva*’ and ‘*peva*’ are the evaluate phases. Table III shows the maximum delay for the tiles of WISP-0 for the NAND-NAND scheme. ‘*hpre*’ and ‘*vpre*’ stand for the horizontal and vertical precharge phases respectively, ‘*heva*’ and ‘*veva*’ are horizontal and vertical evaluate phases. All delays are in picoseconds.

The horizontal phases of both the schemes are identical, since the transistors are of the same type and similar coupling scenarios exist. The vertical planes of the NAND-NAND scheme are significantly faster than those in the OR-plane owing to the much lower ON

TABLE I. PARAMETER VALUES

NW Pitch	10nm
Channel Length of NW Transistors (<i>l</i>)	5nm
Width of NW Transistors (<i>w</i>)	4nm
Oxide Thickness (<i>t_{ox}</i>)	1nm
Dielectric Constant of SiO ₂ (ϵ_r)	2.2
p-type NW ON Resistance (R_{ON-P})	7.875 k Ω
n-type NW ON Resistance (R_{ON-N})	3.75 k Ω
Resistivity of NiSi (ρ_{NiSi})	10^{-5} Ω -cm

TABLE II. AND-OR DELAY (ps)

	<i>ndis</i>	<i>neva</i>	<i>ppre</i>	<i>peva</i>
PC	0.056	0.177	0.045	0.415
ROM	0.047	0.480	0.163	6.015
DEC	0.154	1.025	0.633	2.327
RF	0.289	1.492	0.501	5.699
ALU	0.153	0.775	0.392	11.138

resistance values for n-type devices. In fact, the delay for the *veva* phase on the tiles of the NAND-NAND scheme, is almost half that of the AND-OR scheme, reflecting the ratio of the ON resistances for the n- and p-type devices. This is to be expected, since the transistor ON resistance is the dominant factor in both schemes; being around two orders of magnitude larger than interconnect resistance.

In WISP-0, datapath lengths and the number of transistors on each datapath are different. Consequently the delay varies over a wide range of values for both the NAND-NAND and AND-OR implementations. However, the performance of a pipeline is determined by the slowest segment; in both cases this is the vertical plane of the ALU - next generation WISP processors would have more balanced pipeline stages. In WISP-0, this delay is 11.138ps for AND-OR and 5.857ps for NAND-NAND. The operating frequency assuming a 33% duty cycle (reflecting a clock needed for a precharge-evaluate-hold control) is easily shown to be 30 GHz for AND-OR and 57 GHz for NAND-NAND. Thus modifications to the CMOS control enable an almost 2X speedup of the circuit as compared to the original version with two types of FETs.

TABLE III. NAND-NAND DELAY (ps)

	<i>hpre</i>	<i>heva</i>	<i>vpre</i>	<i>veva</i>
PC	0.056	0.177	0.032	0.231
ROM	0.047	0.480	0.106	2.955
DEC	0.154	1.025	0.475	1.512
RF	0.289	1.492	0.380	3.315
ALU	0.153	0.775	0.304	5.857

5.3 Defect Tolerance

Previously proposed NASIC fault techniques such as built-in redundancy, error correction circuits, and system-level CMOS voting are applicable to the new schemes, so defect-resilient logic can be constructed

using a single type of FET. In addition, it is expected that these techniques will be equally effective since the NW grids, where defects may be possible, are completely unchanged, and the CMOS support is assumed to be defect free. Detailed review of defect tolerance techniques is beyond the scope of this paper.

5.4 Manufacturing Aspects

It has been reported that complementary doping on silicon NWs creates devices with inherently different electrical transport properties such as transconductance and carrier mobility [6]. With the new control scheme such device constraints are removed. This is especially important because of scaling. When assembling large designs, using differently doped NWs in different dimensions is more complicated than using a single type in both dimensions. The new scheme may facilitate the use of some manufacturing techniques, such as those based on soft lithography and patterning that were previously difficult due to the requirement for dissimilar NWs [13]. This scheme does not impose any additional metallization or alignment constraints compared to the original one.

From a manufacturing perspective, the elimination of dissimilar devices appears to be a pure win. There are no disadvantages and we can see several advantages.

6. Conclusions

This paper has shown that it is possible to design nanoscale logic circuits using only one type of FET in the nanoscale portions with no degradation of performance, defect-masking or density. In fact, the performance can be improved by close to 2X would only n-type devices used. In addition, this work is a significant step towards reducing manufacturing requirements. Combined with built-in fault-tolerance techniques it is an interesting direction to explore in building new nanoscale computing systems.

7. References

[1] C.A. Moritz, *et al*, "Fault-Tolerant Nanoscale Processors on Semiconductor Nanowire Grids", *IEEE Transactions on Circuits and Systems I*, vol 54, pp. 2422-2437, 2007.

[2] C. A. Moritz and T. Wang, "Towards Defect-Tolerant Nanoscale Architectures", *Sixth IEEE Conference on Nanotechnology, IEEE Nano2006*, vol 1, pp. 331-334, 2006.

[3] A. DeHon. "Nanowire-based programmable architectures", *ACM Journal on Emerging Technologies in Computing Systems*, vol 1, pp. 109-162, 2005.

[4] C. A. Moritz and T. Wang, "Latching on the wire and pipelining in nanoscale designs", *Non-Silicon Computing Workshop, NSC-3*, 2004.

[5] T. Wang, M. Bennaser, Y. Guo, and C. A. Moritz, "Self-healing wire-streaming processors on 2-d semiconductor nanowire fabrics", *Nanotech 2006, Nano Science and Technology Institute*, 2006.

[6] W. Lu and C.M. Lieber, "Semiconductor Nanowires", *J. Phys. D: Appl. Physics*, vol. 39, pp. R387-R406, October 2006.

[7] Y. Cui, X. Duan, J. Hu, and C. M. Lieber, "Doping and Electrical Transport in Silicon Nanowires", *Journal of Physical Chemistry B*, vol. 104, pp. 5213-5216, May 2000.

[8] Y. Huang, X. Duan, Q. Wei, and C. Lieber, "Directed assembly of one-dimensional nanostructures into functional networks", *Science*, vol. 291, pp. 630-633, 2001.

[9] D. Whang, S. Jin, Y. Wu, and C. M. Lieber. "Large-scale hierarchical organization of nanowire arrays for integrated nanosystems". *Nanoletters* vol 3, pp. 1255-1259, September 2003.

[10] A. B. Greytak, L. J. Lauhon, M. S. Gudiksen, and C. M. Lieber, "Growth and transport properties of complementary germanium nanowire field-effect transistors", *Applied Physics Letters*, vol. 84, pp. 4176-4178, May 2004.

[11] Y. Wu, J. Xiang, C. Yang, W. Lu, C. M. Lieber, "Single-crystal metallic nanowires and metal/semiconductor nanowire heterostructures", *Nature*, vol. 430, pp. 699-703, 2004.

[12] H. T. Ng, J. Han, T. Yamada, P. Nguyen, Y. P. Chen, and M. Meyyappan, "Single Crystal Nanowire Vertical Surround-Gate Field-Effect Transistor", *Nano Letters*, vol. 4, pp. 1247-1252, 2004.

[13] B. D. Gates, Q. Xu, J. C. Love, D. B. Wolfe, and G. M. Whitesides, "Unconventional Nanofabrication", *Annu. Rev. Mater. Res.* 2004, vol. 34, pp. 339-372, 2004.

[14] J. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits – A Design Perspective*, 2nd Ed. Upper Saddle River, NJ: Prentice-Hall 2003