CMOS CONTROL ENABLED SINGLE-TYPE FET NASIC

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Abstract **A new hybrid CMOS-nanoscale circuit style has been developed that uses only one type of Field Effect Transistor (FET) in the logic portions of a design. This is enabled by CMOS providing control signals that coordinate the operation of the logic implemented in the nanoscale. In this paper, the new circuit style is explored, examples from a microprocessor design are shown, manufacturing and density implications discussed. The system is based on the existing CMOS-nano hybrid fabric architecture NASIC, but the new circuit style reduces the requirements on devices and manufacturing from previous NASIC designs, significantly improves performance without any deterioration in circuit density.**

Index Terms **— Semiconductor Nanowires, Nanofabrics, NASIC, Nanoscale Processors**

I. Introduction

Semiconductor nanowires are a promising nanodevice technology, but there are some major challenges to overcome before systems built out of these devices can become a reality. The primary issue is the manufacturability of architectures. It is difficult to reliably construct nanowire-based systems with good performance characteristics due to both device and manufacturing-related concerns. Therefore, one of the objectives of any nanoscale fabric architecture is to minimize underlying manufacturing and device requirements.

For instance, in designs based on semiconductor nanowires, it is difficult to build both p- and n-FETs using the same material. While complementary FETs have been demonstrated in zinc oxide [19], silicon [11], and germanium [16] nanowires, in all cases large differences in transport properties were found between the two types of FETs, sometimes much greater than those seen in today's traditional CMOS transistors. As the transistor characteristics are certain not to be symmetric between n-FETs and p-FETs, this would make timing closure more complicated thereby making it harder to manufacture systems reliably. Consequently, when designing at the nanoscale, it would be advantageous if only one type of device were required.

However, in general, conventional logic systems designed using mostly one type of FETs, such as pseudo-NMOS, suffer from major power and performance drawbacks as compared to CMOS [21]. This is one reason why such designs have not found widespread applicability.

By using a fabric style that combines CMOS support with nanoscale logic implementation, these problems can be eliminated. First, instead of using a design style such as pseudo-NMOS, the control scheme may be moved into CMOS and the design modified such that the associated nanoscale circuits could function with only one type of FET. Furthermore, by adopting in conjunction a dynamic scheme for the nanoscale logic, the leakage power consumption can be minimized by eliminating direct paths between ground and the power supply voltage.

In the techniques presented in this paper, a dynamic NMOS logic style is shown with clock signals generated in CMOS. The new design style is demonstrated with several circuit examples and a streaming processor design. It does not incur any density penalty as compared with similar design styles using complementary devices and improves circuit speeds by close to 2X. In a similar way, a PMOS logic scheme could also be developed. A PMOS version would have the same density but inferior performance compared to the NMOS design.

The rest of the paper is organized as follows. An overview of the NASICs fabric architecture is presented in Section II and the new design style is discussed in Section III. Single-type FET implementation of WISP-0, a NASIC processor, is shown in Section IV. Section V contains some analysis and evaluation of systems using the single-type FET scheme. Conclusions are presented in Section VI.

II. Overview Of Nasics

It is possible, with self-assembly techniques, to produce arrays of doped nanowires with nanometer pitches. These can then be placed at right angles with each other, forming a grid [14]. Depletion mode FETs can be formed at the crosspoints.

NASIC (Nanoscale Application Specific Integrated Circuit) is a fabric architecture based on these sorts of semiconductor nanowire grids with FETs at certain crosspoints

[1][2][5][6][7][8][9]. The nanowires are connected to microwires which provide control signals generated from CMOS circuitry. The nanowire grids are laid out in tiles, with each tile implementing two-stage logic with a dynamic control style that channels the flow of data through these tiles.

Previous NASIC implementations have been based on a 2-level AND-OR logic style, involving both n- and p-type FETs. These designs are self-healing: defects are masked using built-in redundancy and error correcting circuits on the nanogrid coupled with system level voting in CMOS. Defect and fault-tolerance are especially important in nano-fabrics where reconfiguration tends to be difficult due to the complex nano-micro interfacing required and the defect rate will likely be very high.

The objective of the NASIC built-in defect-tolerance is to have masking for permanent defects, transient faults due to parameter variation and noise. This also helps with the additional noise challenges introduced by using dynamic logic. For clarity of the explanation of logic operation, the defect tolerance techniques are omitted in all following diagrams and explanations. The focus instead is on the new control and circuit scheme and its implications. The fault tolerance techniques as discussed in [1][2] are directly applicable to the new design style.

In order to provide the reader with an insight into the NASIC fabric architecture, following is a detailed description of the functioning of a NASIC tile.

Fig. 1 illustrates the design of a 1-bit NASIC full adder in a dynamic style with two types of FETs required for AND-OR logic implementation. Each nanotile is surrounded by microwires (MWs), which carry V_{dd} and V_{ss}. Other microwires carry the control signals generated by CMOS, but these are not shown in this diagram. Instead, the labels *ndis1*, *ndis2*, *neva1*, *neva2*, *ppre1*, *ppre2*, *peva1* and *peva2* represent the nanowires connected to these control microwires. The lines suffixed with '2' are control wires for the next adjacent tile which, as will be seen later, needs to be coordinated with this tile to meet hold-time constraints. The *dis* and *pre* lines are for predischarge and precharge, respectively. The *eva* lines trigger logic evaluation.

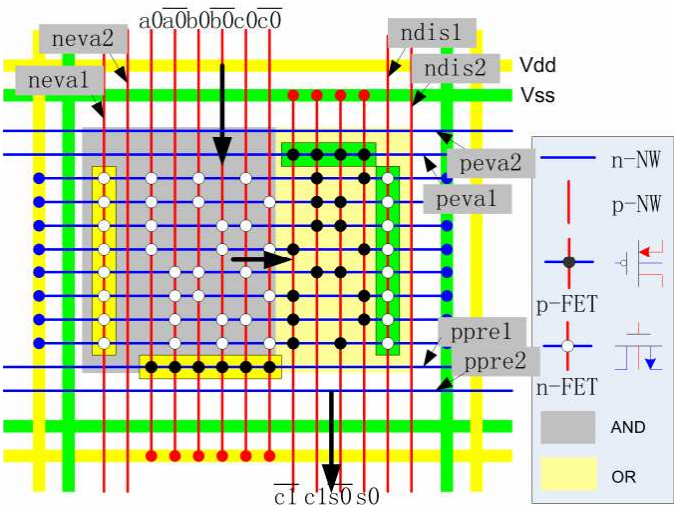

Figure 1 Dynamic implementation of a 1-bit full adder in NASIC. The thicker wires represent microwires (MWs) and the thin ones are NWs. The doping type of the wires (p-type or n-type) along source-drain of a FET transistor determines the type of the transistor. The black and white dots, at the crosspoints of NWs, represent p-FETs and n-FETs respectively. The function is based on AND-OR logic. Arrows show propagation of data through the tile.

This tile implements AND-OR logic as a canonical sum-of-products. The left portion selectively ANDs together the inputs, depending on whether a transistor is present for that input on each row, and generates midterms. The right side implements OR logic on these midterms to form the final outputs for the tile. The tile can thus be said to be divided into AND and OR planes.

The inputs flow in from the top, and the outputs flow out from the bottom, on the labeled wires. In multi-tile NASIC designs, NWs are used to provide communication between adjacent tiles, while some global signals are routed through CMOS.

Dataflow in NASICs is through a 3-phase progression. The CMOS control signals are responsible for the coordination of these phases.

Phase1: *ndis1* (predischarge n-type nanowires) is switched on. This gates the right side of all the horizontal nanowires to V_{ss}.

Phase2: *ndis1* is switched off and the AND logic plane is evaluated by turning on *neva1*. For example, if the inputs are 111, the horizontal NW gated by a0, b0 and c0 is pulled to V_{dd}. All other NWs will retain logic '0'. Simultaneously, the OR plane, consisting of vertical output p-type NWs running out of the bottom of the tile is precharged to V_{dd}.

Phase 3: During phase 3, *ndis1* and *neva1* signals are switched off, and the values evaluated on the horizontal NW in the previous phase are held. These horizontal nanowires gate the transistors on the OR plane. The OR Plane consisting of p-type nanowires is evaluated (*peva1* transistors are ON) and the outputs generated. The OR plane must now hold its output for an additional phase, having neither *ppre1* nor *peva1* turned on, so that the next tile can use this output as its input. The control of each adjacent tile is hence offset in time from the previous one. For example, the successor tile is evaluating its AND plane while the current OR plane is in the HOLD phase. Thus, the synchronous switching of control signals generated from CMOS coordinates the evaluation and flow of data through multiple logic tiles in a NASIC fabric.

A. NASIC Manufacturing

Manufacturing of NASICs may be achieved through a combination of self-assembly and conventional top-down manufacturing steps.

- Growth and Alignment of Nanowires: NWs can be grown using seed catalyst techniques or other methods

that may ensure uniform nanowire diameters [11]. During growth NWs may be lightly doped for semiconductivity. NWs may be aligned into parallel horizontal and vertical sets with Langmuir-Blodgett techniques. Other approaches based on soft lithographic techniques [14] or di-block polymers may also be possible.

- Metallization using lithographic mask: Regions on individual nanowires where there should be no FET channels will then need to be metallized with the help of a lithographic mask. Though a 2NW pitch resolution is required, precise shaping is not needed, making this step less challenging as compared to a CMOS manufacturing step for a similar feature size.
- An oxide layer may then be grown over the gate regions of the nanowires and a 2D grid formed by moving one NW set on top of the other.
- A fine grain metallization step is needed to demarcate FET channels, create metallic interconnect between neighboring FETs, and extend the metallic regions created in the previous metallization step. This fine grain metallization may be achieved by using the top NW as a self-aligning mask as shown in [15].
- Micro-Nano interfacing may be done in conjunction with lithographic process steps.

Although many of the key individual steps required have been demonstrated, combining the necessary steps for reliable manufacturing remains a challenging and unproven process.

III. NASICS WITH SINGLE-TYPE FETS

A. Modifications to the control scheme

It has been found that altering the CMOS control scheme obviates the need for two types of devices to implement arbitrary logic functions on the nanogrid. The scheme may thus be used with manufacturing processes where complementary devices are difficult or impossible to achieve. A design using only n-type FETs will implement a NAND-NAND cascaded logic whereas a design using p-type FETs will implement a NOR-NOR logic. Fundamentally, these are equivalent with the

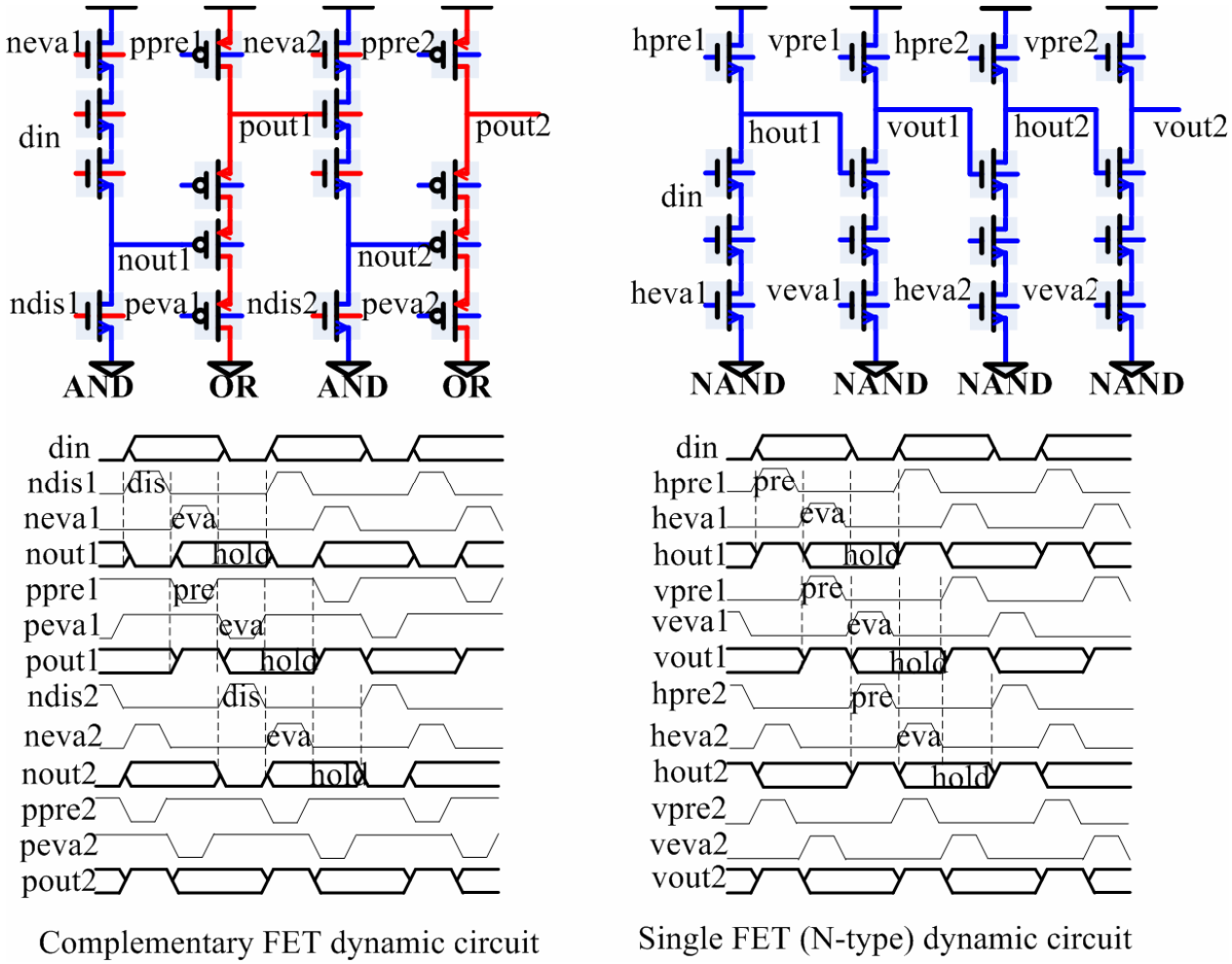

Figure 2. Timing diagrams of AND-OR (complementary FET) and NAND-NAND (n-type FET) dynamic circuit designs.

original AND-OR.

Fig. 2 compares the timing diagrams of cascaded AND-OR (original) and NAND-NAND (proposed) schemes over 2 successive nanotiles. The control signals for the latter are horizontal and vertical precharge (*hpre1,2* and *vpre1,2*) as well as evaluate signals (*heva1,2* and *veva1,2*). The '*n*' and '*p*' prefixes have been dropped since only one type of nanowire is used. The dynamic 3-phase scheme of precharge, evaluate and hold is still in place. However the behaviour of the control signals has been modified. Firstly, there are no predischarge phases, all planes are precharged since successive planes implement the same kind of logic function (NAND in this case). Also, all control signals are active high, since they gate n-type FETs.

B. *Implementation with n-type devices*

Fig. 3 shows a 1-bit full adder built using only n-type devices. Its function is very similar to the circuit with complementary devices. Note that the connections to V_{dd} and V_{ss} (yellow and green MWs) have been changed relative to the previous design for the horizontal plane.

In comparison with the previous implementation it may be noted that the relative positions of the transistors in the NAND-NAND example is identical to the AND-OR implementation. Fig. 4 shows a diagram of the logic function of a single nanowire for various wirings and devices. As seen from the diagram, the only change from AND to NAND is in the swapping of the control signals, V_{dd} and V_{ss}. The output node is precharged rather than predischarged which results in the inversion of the function.

On the vertical plane, the change is more significant: from OR to NAND. In this case both the type of the transistor as well as the polarity of the control scheme has been changed. Also, the inputs to the vertical NW are now inverted from their values in the AND-OR scheme. The inversion of the inputs in conjunction with the change from OR to NAND – results in a transformation of the logic function being performed. De Morgan's Laws tell us that this transformation should produce the same result as the AND-OR scheme. This allows us to maintain the transistors in their original positions, even though the logic functions used have changed. It can thus easily be seen that there will be no impact on the area of the nanotile itself. In addition, the new scheme also reduces the number of microwires by using the same function and consequently the same polarity for multiple control signals, thus allowing them to share some microwires.

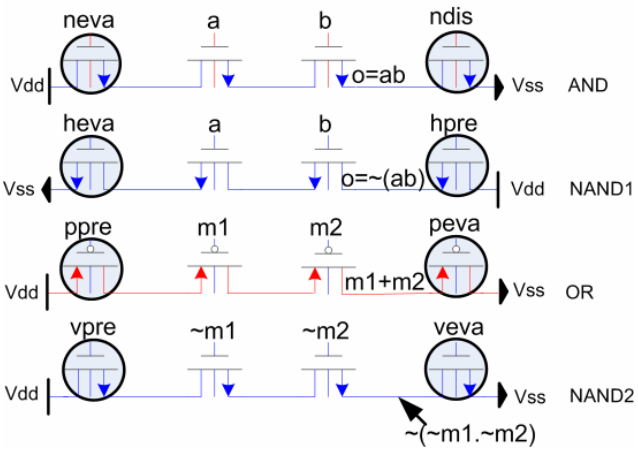

Figure 4. Transistor positions: Stage by stage comparison of the AND-OR and NAND-NAND logic styles. 'm' signals represent midterms, signals prefixed by '~' are complements.

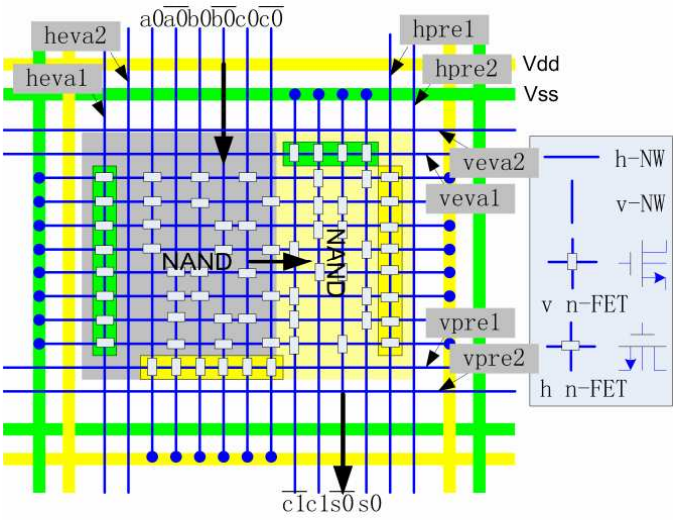

Figure 3. n-FET only implementation of 1-bit adder using the proposed NAND-NAND cascaded scheme. The FET channel is oriented along the length of the rectangle in both horizontal and vertical nanowires in the figure. Arrows show propagation of data through the tile.

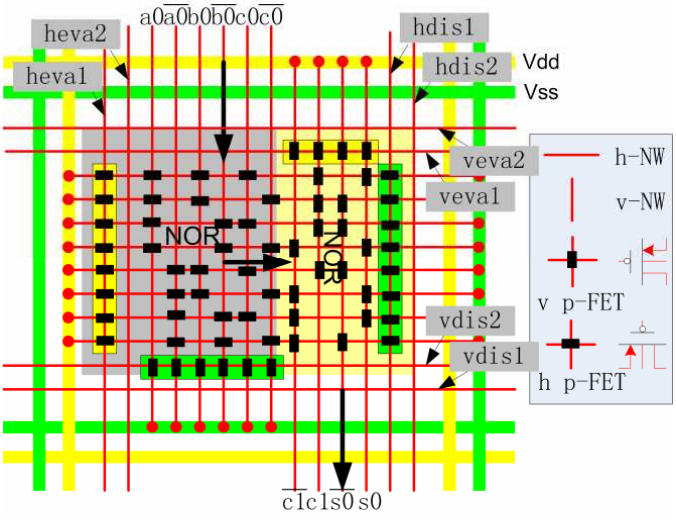

Figure 5. Single FET implementation of 1-bit adder using p-type devices and NOR-NOR cascaded scheme. The channel is oriented along the length of the rectangle in both horizontal and vertical nanowires. Arrows show propagation of data through the tile.

C. *Implementation with p-type devices*

Fig. 5 shows the equivalent implementation of the adder using p-type devices. The control scheme for this circuit uses predischarge (*vdis1* and *hdis1*) and evaluate (*heva1* and *veva1*) signals. All control signals are active low in this case. The circuit is implemented with two NOR planes. Once again the relative positions of the transistors is identical to the AND-OR and NAND-NAND logic schemes.

IV. Single-Type FET Implementation Of WISP-0

WISP-0 is a stream processor that implements a 5-stage microprocessor pipeline architecture including *fetch, decode, register file, execute* and *write back* stages [5]. WISP-0 consists of five nanotiles. Fig. 6 shows its layout. A nanotile is shown as a box surrounded by dashed lines in the figure. In WISP designs, in order to preserve the density advantages of nanodevices, data is streamed through the fabric with minimal control/feedback paths. It uses dynamic circuits and pipelining on the wires to eliminate the need for explicit flip-flops and therefore improve the density considerably.

In this section, WISP-0 implementation using the new logic style is demonstrated.

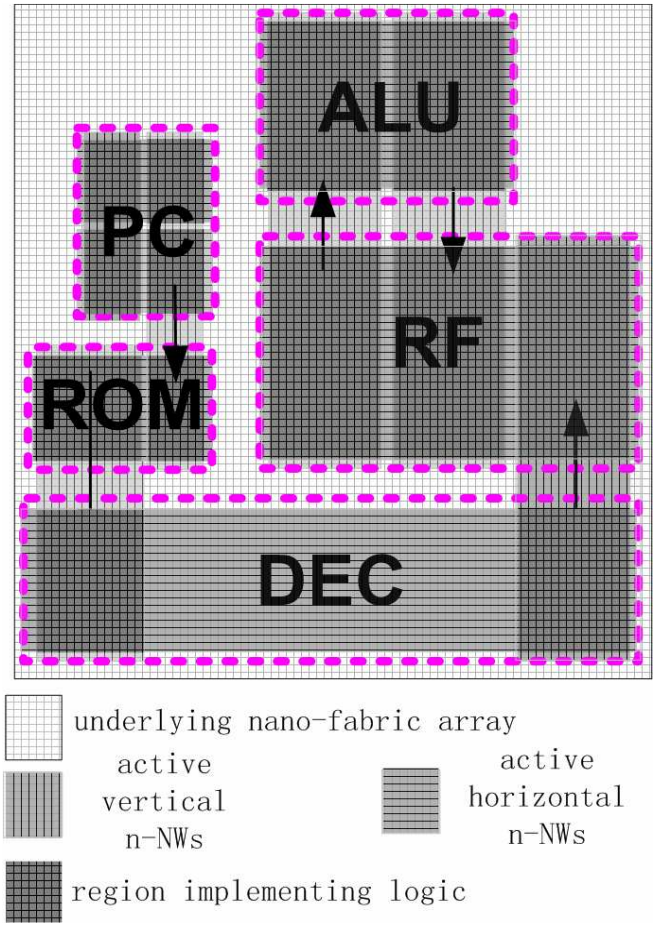

Figure 6. WISP-0 Floorplan

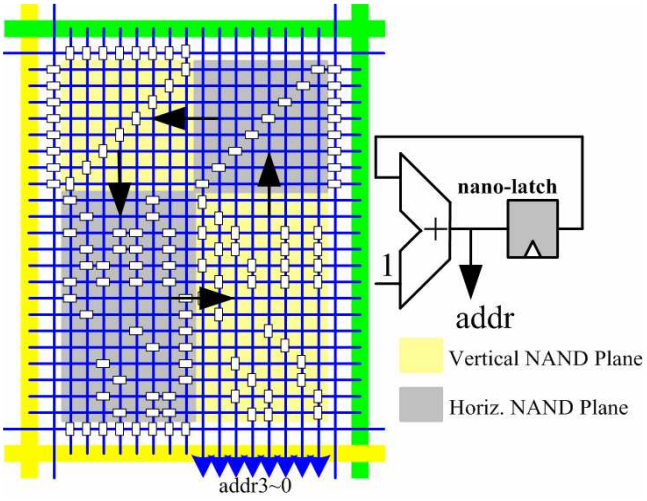

Figure 7. Layout and Schematic of the WISP-0 Program Counter with n-FETs in both horizontal and vertical directions

A. *WISP-0 Program Counter*

The WISP-0 program counter is implemented as a four bit accumulator. Its output is a four bit address that acts as an input to the ROM. The address is incremented each cycle and fed back using a nano-latch. Fig. 7 shows the implementation of the Program Counter with a NAND-NAND scheme. Diagonal transistors on the two upper two NAND planes implement the nano-latch to delay the output by one cycle and allow the signals to 'turn the corner' [5].

B. *WISP-0 ROM*

The WISP-0 ROM may store up to 16 7-bit instructions. Fig. 8 shows the implementation of the ROM using the new scheme. The ROM receives a four bit address from the program counter and outputs a 7 bit instruction which is fed into the decoder. The address for each instruction is held in the right-hand logic plane while the bits making up the instruction itself are in the left-hand plane. The address plane will set only one of the horizontal wires to logic '1', thus selecting a single instruction to output.

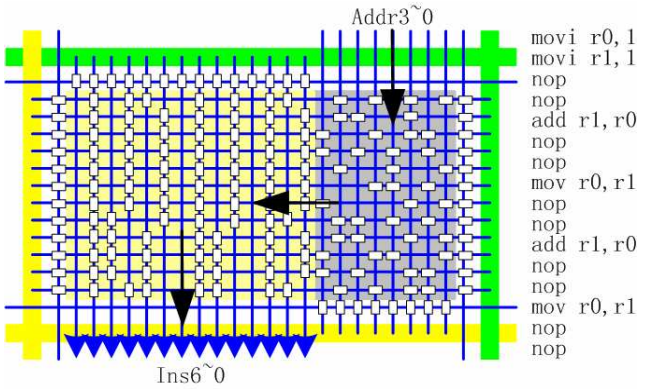

Figure 8. Layout and schematic of a WISP-0 ROM with n-type horizontal and vertical nanowire FETs.

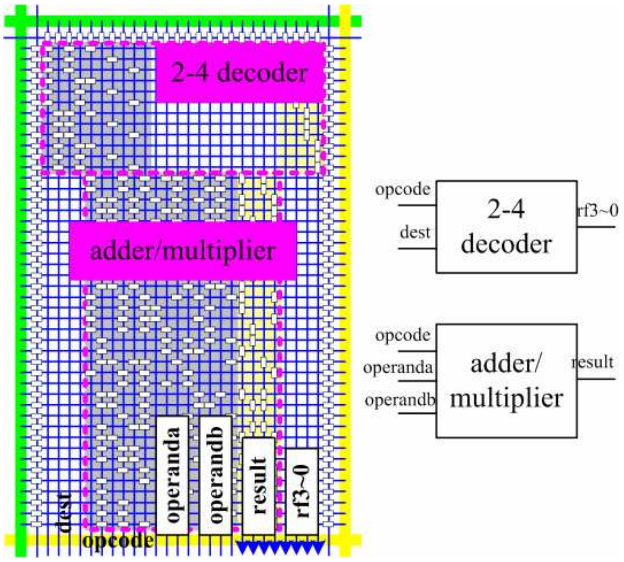

Figure 9. Layout and schematic of a WISP-0 ALU with n-type horizontal and vertical nanowire FETs.

C. *WISP-0 Arithmetic Logic Unit*

Fig. 9 shows the layout and schematic of the WISP-0 ALU that implements both addition and multiplication functions. The arithmetic unit integrates an adder and multiplier together to save area. It takes the inputs (at the bottom) from the register file and produces the write-back result. At the same time, the write-back address is decoded by the 2-4 decoder on the top and transmitted to the register file along with the result. The result will be written to the corresponding register in the next cycle.

V. DISCUSSION

A. *Density Evaluation*

As shown in the logic diagrams, the nanowire portion of the area will not change at all, as the transistors are laid out in exactly the same way as in the circuits with two types of transistors. A useful by-product of using a single-type of FET though is a reduction in the number of microwires due to the modifications to the control scheme that allows sharing of some CMOS signals. Reduction in the number of microwires is a density advantage, since microwires have a significant area overhead, even at end-of-roadmap feature sizes. The actual benefit would depend on the size of the design – larger designs, where the microwire area is small in comparison to the logic portions, will benefit less.

Fig. 10 compares the normalized densities of the two logic schemes against CMOS implementation of WISP-0 for various technology nodes. Nanowire pitch is assumed to be 10nm whereas microwires are assumed to be separated by the minimum wire pitch for the respective technology according to the ITRS Roadmap.

Due to the sharing of some signals, the NAND-NAND logic

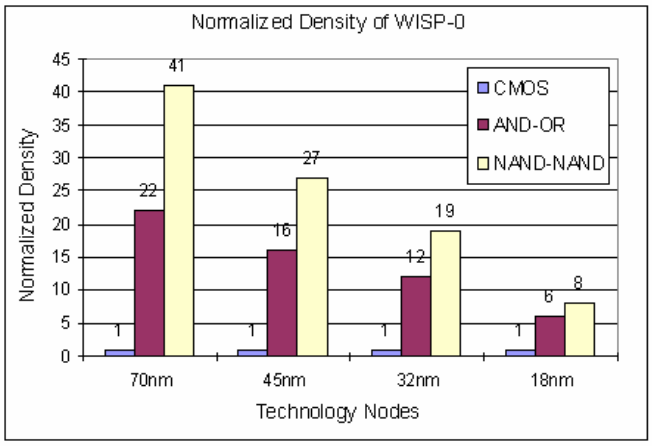

Figure 10. Comparison of Normalized densities against CMOS implementation of WISP-0 for different technology nodes

requires 7 surrounding microwires per tile as opposed to the AND-OR scheme which requires 10. For the 32 nm node this corresponds to an area improvement close to 37% whereas for the 18nm technology this is 25%.

Microwires make up a significant part of the area, especially in the larger nodes. Despite this overhead, NASIC is denser than CMOS because all logic is implemented on the nanowire grid. CMOS still must pay the same overhead for control while also requiring much larger area for logic implementation. For more information about relative densities of NASICs with various defect-tolerance techniques, please see [1][2][8].

B. *Performance Evaluation*

With schemes such as AND-OR, the performance of the circuit will be limited by the cascaded planes employing the slower devices. Also, since arbitrary sizing of devices on the nanogrid is not achievable, it is not possible to match the performance characteristics of dissimilar devices. Therefore elimination of the slower devices using the new control scheme carries significant performance benefits, despite the fact that the transistors are laid out in exactly the same fashion.

Delay estimation has been done for the tiles of WISP-0 for both the AND-OR and NAND-NAND logic implementations. A nanowire pitch of 10nm, an oxide layer thickness of 1nm, and a dielectric constant of 2.2 were assumed. The p-type devices for this evaluation are Silicon Nanowires (SiNW) lightly doped with Boron. The n-type devices are SiNW lightly doped with Phosphorous. Nanowire transistor length is 5nm and width is 4nm. The ON resistance for these geometries for the two types of devices ($R_{ON\text{-}P}$ and $R_{ON\text{-}N}$) has been calculated to be 7.875 kΩ and 3.75 kΩ respectively based on experimental work reported in [10]. The interconnect is created using a Nickel based metallization process, and the resistivity of the NiSi thus formed is assumed to be 10^{-7} Ω-m [18]. The contact resistance is ignored in order to assess the true performance impact of migrating to the single-FET scheme. Table II summarizes all parameter values.

TABLE I. PARAMETER VALUES

NW Pitch	10nm
Channel Length of NW Transistors (l)	5nm
Width of NW Transistors (w)	4nm
Oxide Thickness (t_{ox})	1nm
Dielectric Constant of SiO_2 (ε_r)	2.2
p-type NW ON Resistance ($R_{ON\text{-}P}$)	7.875 kΩ
n-type NW ON Resistance ($R_{ON\text{-}N}$)	3.75 kΩ
Resistivity of NiSi (ρ_{NiSi})	10^{-5} Ω-cm

1) Delay Calculations

A lumped RC model is used for the worst-case delay analysis. Expressions from [3] were used for capacitance estimation. These calculations take into account NW-NW junction capacitances and relatively realistic coupling scenarios. The coupling capacitance per unit length was found to be 39.04pF/m. The junction capacitance was found to be 0.652aF.

Table II indicates the capacitive loading on each tile of WISP-0 for different clock phases. Since capacitance depends only on the device geometries and the dielectric medium and not on the type of device, these values are identical for both logic schemes.

During each phase, there is one control NW and one or more datapath NWs switching. In the table 'Control NW (H)' refers to a Horizontal precharge/evaluate signal. Since the precharge and evaluate control NWs in one plane are geometrically identical, the capacitive loading on these NWs is the same. 'Datapath NW (V)' refers to datapath nanowires in the vertical plane. The capacitive loading during precharge and evaluate is dissimilar for datapaths owing to different lengths and coupling effects.

The lumped capacitance is in the range of ado-Farads, and as expected, larger components such as the RF (Register File) are more heavily loaded. Table III shows the maximum delay for the tiles of WISP-0 for the AND-OR scheme. '*ndis*' and '*ppre*' stand for the n- device discharge and p-device precharge phases respectively, '*neva*' and '*peva*' are the evaluate phases. All delays are in picoseconds.

TABLE II. CAPACITIVE LOADING (ado-Farads)

	Control NW(H)	**Datapath NW(H)**		**Contral NW (V)**	**Datapath NW(V)**	
	pre/eva	***pre***	***eva***	***pre/eva***	***pre***	***eva***
PC	14.99	9.78	25.27	11.08	4.56	32.43
ROM	8.48	11.08	33.47	9.78	20.12	82.68
DEC	11.74	20.21	83.33	11.74	42.38	143.1
RF	27.38	26.73	98.21	9.13	42.48	167.6
ALU	29.34	18.26	37.78	16.95	30.64	138.7

TABLE III. DELAY (picoseconds) – AND-OR LOGIC

	ndis	**neva**	**ppre**	**peva**
PC	0.056	0.177	0.045	0.415
ROM	0.047	0.480	0.163	6.015
DEC	0.154	1.025	0.633	2.327
RF	0.289	1.492	0.501	5.699
ALU	0.153	0.775	0.392	11.138

TABLE IV. DELAY (picoseconds) – NAND-NAND LOGIC

	hpre	**heva**	**vpre**	**veva**
PC	0.056	0.177	0.032	0.231
ROM	0.047	0.480	0.106	2.955
DEC	0.154	1.025	0.475	1.512
RF	0.289	1.492	0.380	3.315
ALU	0.153	0.775	0.304	5.857

Table IV shows the maximum delay for the tiles of WISP-0 for the NAND-NAND scheme. '*hpre*' and '*vpre*' stand for the horizontal and vertical precharge phases respectively, '*heva*' and '*veva*' are horizontal and vertical evaluate phases. All delays are in picoseconds.

The horizontal phases of both the schemes are identical, since the transistors are of the same type and similar coupling scenarios exist. The vertical planes of the NAND-NAND scheme are significantly faster than those in the OR-plane owing to the much lower ON resistance values for n-type devices. In fact, the delay for the *veva* phase on the tiles of the NAND-NAND scheme, is almost half that of the AND-OR scheme, reflecting the ratio of the ON resistances for the n- and p-type devices. This is to be expected, since the transistor ON resistance is the dominant factor in both schemes; being around two orders of magnitude larger than the NiSi interconnect resistance.

In WISP-0, datapath lengths and the number of transistors on each datapath are different. Consequently the delay varies over a wide range of values for both the NAND-NAND and AND-OR implementations. However, the performance of a pipeline is determined by the slowest segment; in both cases this is the vertical plane of the ALU - next generation WISP processors would have more balanced pipeline stages. In WISP-0, this delay is 11.138ps for AND-OR and 5.857ps for NAND-NAND. The operating frequency assuming a 33% duty cycle (reflecting a clock needed for a precharge-evaluate-hold control) is easily shown to be 30 GHz for AND-OR and 57 GHz for NAND-NAND. Thus modifications to the CMOS control enable an almost 2X speedup of the circuit as compared to the original version with two types of FETs.

C. Defect Tolerance

Previously proposed NASIC defect and fault techniques such as built-in redundancy, error correction circuits, and system-level CMOS voting are applicable to the new schemes, so defect-resilient logic can be constructed using a single type of FET. In addition, it is expected that these techniques will be equally effective. This is because the nanowire grids, where defects may be possible, are completely unchanged, and the CMOS support is assumed to be defect free. Detailed review of these defect tolerance techniques is beyond the scope of this paper.

D. Manufacturing Aspects

It has been reported that complementary doping on silicon nanowires creates devices with inherently different electrical transport properties such as transconductance and carrier mobility [11]. This has been an important issue in building logic families using nanowire fabrics.

With the new control scheme device constraints are reduced because of the requirement for only a single type of FET. This is especially important because of scaling. When assembling large designs, using differently doped nanowires in different dimensions is more complicated than using a single type in both dimensions. The new scheme may also facilitate the use of some manufacturing techniques, such as those based on soft lithography and patterning that were previously difficult due to the requirement for dissimilar nanowires [20].

This scheme does not impose any additional metallization or alignment constraints compared to the original one. It should be possible to use the same methods as used for NASICs with two types of transistors.

From a manufacturing perspective, the elimination of dissimilar devices appears to be a pure win. There are no disadvantages and we can see several advantages.

VI. CONCLUSIONS

This paper has shown that it is possible to design nanoscale logic circuits using only one type of FET in the nanoscale portions with no degradation of performance, defect-masking or density. In fact, the performance can be improved by close to 2X would only n-type devices used. In addition, this work is a significant step towards reducing manufacturing requirements. Combined with built-in defect- and fault-tolerance techniques it is an interesting direction to explore in building new nanoscale computing systems.

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