Towards Automatic Thermal Network Extraction in 3D ICs

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ABSTRACT
Thermal management is one of the critical challenges in 3D integrated circuits. Incorporating thermal optimizations during the circuit design stages requires a convenient automatic method of doing thermal characterization for feedback purposes. In this paper, we present a methodology, which supports thermal characterization by automatically extracting the steady-state thermal modeling resistance network from a post-placement physical design. The method follows a two-level hierarchical approach. It does fine-grained thermal modeling for standard cells, and then at higher level assembles the thermal modeling network of the input physical design by using the built standard cell thermal models, and adding the information on inter-cell connections as well as implemented thermal management features. The methodology has been implemented in Skybridge-3D-CMOS technology, but can be employed in other fine-grained 3D directions such as monolithic 3D CMOS. Large scale benchmarking has been performed, showing the ability of doing automated fine-grained thermal characterization in the order of seconds per thousands of 3D standard cells. In addition, the methodology is employed to highlight implications of added thermal extraction features.

CCS Concepts
• **Hardware → Emerging technologies**

Keywords
3D heat management; thermal modeling network extraction; Skybridge; Skybridge-3D-CMOS

1. INTRODUCTION
3D integration is an emerging technology to enable surpassing many of the current limitations in traditional CMOS scaling [1]-[4]. However, the thermal problem is a critical challenge in 3D integrated circuits (ICs) due to the higher transistor density and worse heat dissipation compared with conventional planar IC [5]-[6]. Researchers have been working on tackling the thermal issues in 3D IC, and thermal-aware CAD is one of the important directions. It incorporates thermal optimizations during various design stages such as floorplanning, placement and routing [7]-[9]. During the optimization, the tool has to repetitively evaluate the design in the thermal domain for feedback, which necessitates a method to support the automatic thermal characterization of large-scale physical designs.

As one of the directions in 3D IC, the Skybridge fabric has been proposed as a vertically-composed fine-grained 3D IC fabric technology, which builds on uniform vertical nanowire templates and utilizes novel assembly, interconnect and heat extraction structures designed with a 3D mindset [10]-[14]. In Skybridge, fine-grained 3D thermal management is supported by incorporating specially-architected intrinsic thermal management fabric components, which allow heat extraction and dissipation from heated regions in the layouts to the substrate, and thus prevent hotspot development. Implementing these thermal features (either manually or with automatic tools) needs automatic thermal characterization. Also, the thermal characterization needs to be able to capture the effects of the intrinsic fabric-level thermal management components in the circuits. Such a circuit-level thermal mitigation mindset, a likely requirement in emerging fine-grained 3D, in conjunction with automated extraction of thermal networks have not been reported yet to the best of our knowledge.

In this paper, we focus on a methodology, which supports the automatic thermal characterization by automatically extracting the steady-state thermal modeling resistance network for a physical design in 3D IC. This methodology employs a hierarchical mindset; at the intra-cell level models the standard cell layouts with detailed analogous thermal modeling circuits, and then at higher level assembles the thermal modeling network for the whole physical design by reusing the built standard cell thermal models. It includes the information on cell placement & routing and thermal features into the modeling network. In particular, it captures the effects of detailed inter-cell routing information as well as the implemented thermal management fabric components in the circuit design. This methodology can apply to various flavors of Skybridge fabrics and other 3D directions including TSV-based and monolithic gate-level / transistor-level 3D IC.

The rest of this paper is organized as follows. In Section II we provide an overview of Skybridge fabric. In Section III we introduce the intrinsic fabric-level heat management features in Skybridge. In Section IV we introduce the proposed methodology of automatic thermal resistance network extraction focusing on the S3DC use case. In Section V we show thermal characterization

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results of several benchmarked S3DC circuits. Section V concludes the paper.

2. SKYBRIDGE FABRIC OVERVIEW

There are several key Skybridge 3D IC directions including Skybridge-Dynamic [10], Skybridge-NP-Dynamic [13] and Skybridge-3D-CMOS (S3DC) [11]. All are based on a uniform vertical pre-doped nanowire template; nanowires are uniformly n-type doped in Skybridge-Dynamic and doped in separate p- and n-type regions in other directions as is shown in Figure 1. The template is later functionalized by multi-layer selective material deposition with no additional doping required. All the Skybridge component structures are designed for 3D manufacturability.

2.1 Skybridge Fabric Components

Skybridge features a true 3D interconnection framework with specifically architected 3D interconnection structures as shown in Figure 2: i) Bridges provide horizontal connections between adjacent nanowires; ii) Coaxial Routing structures carry signals vertically along nanowires; iii) nanowires can be used for vertical routing since they are heavily-doped and silicided and thus have good conductivity; iv) Skybridge-Interlayer-Connection (SB-ILC) [11] provides good Ohmic contact between various doping regions of a nanowire (detailed structure and chosen materials shown and explained in Figure 2(B)). S3DC overcomes a key challenge in creating CMOS circuits with pull-up and pull-down networks in vertical dimension.

Uniform Vertical Gate-All-Around (V-GAA) Junctionless transistor acts as the active device in Skybridge fabrics; an n-type transistor structure is shown in Figure 3. The device behavior is modulated by the work function difference between gate electrodes and the channels. The concept of this type of transistors has been well researched [15], and also experimentally demonstrated [16]. Although Junctionless devices are often considered as providing lower on-current and somewhat worse device-level performance, in Skybridge it is a part of a fine-grained 3D integration solution, with dense connections and design, that overall yields higher performance at the fabric-level despite a somewhat sub-optimal device vs state-of-the-art FinFETs.

2.2 Skybridge Circuits

Various directions in Skybridge fabrics support different circuit styles. Figure 4 shows an S3DC three-input NAND gate which follows the static CMOS circuit style. Three parallel p-type transistors on the top p-doped region act as the pull-up network and three serial n-type transistors at the bottom as the pull-down network. SB-ILC connects the pull-up and pull-down circuits to generate the output signal, which is conducted out by Bridges. The functionality of the circuits have been verified through detailed HSPICE simulations in physical level. For more details please refer to [10]-[11].

3. S3DC HEAT MANAGEMENT

In order to tackle the heat management challenge in fine-grained 3D, Skybridge fabrics have incorporated intrinsic thermal management fabric components including Heat Extraction Junctions (HEJs), Heat Extraction Bridges (HEBs), and Heat Dissipating Power Pillars (HDPPs). Instead of following the conventional mindset which only incorporates heat management considerations during the IC design cycle, it employs fabric-level heat management support that can be employed at the circuit level when needed. An overview of all the thermal management components are shown in Figure 5.

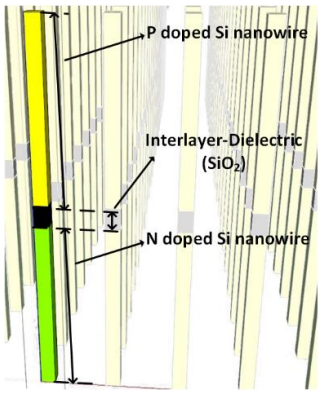

Figure 1. Uniform vertical nanowire template.

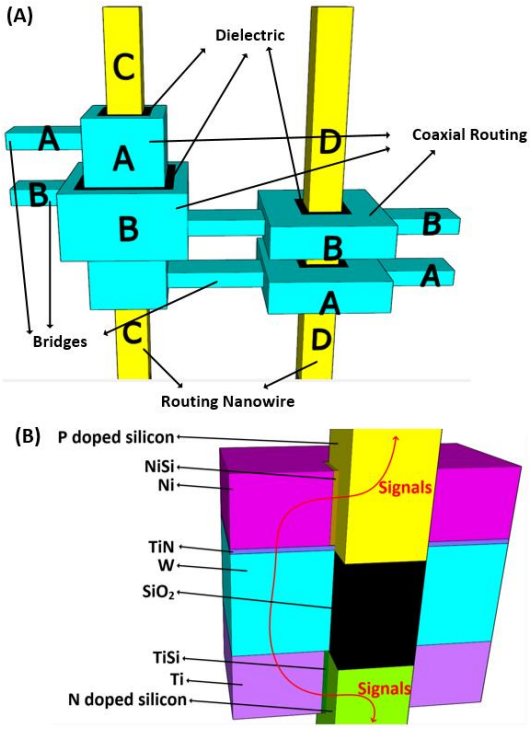

Figure 2. S3DC interconnection components: A). 3D connections within one doping layer realized by Bridges, Coaxial Routings, and routing nanowires; B). SB-ILC allows routing between various doping layers without

(i). HEJs are specialized junctions that are designed for extracting heat from hot spots on logic nanowires. The material types are chosen so that they are good at thermal conduction without interfering with the normal circuit operations.

(ii). HEBs are similar with the signal-carrying Bridges, but they are only designed to connect HEJs on one end and HDPPs on the other. They provide good lateral heat dissipating paths.

(iii). HDPPs serve the purpose of both power supply and heat dissipation. These pillars are built with Tungsten and large in area (2x2 nanowire pitch), and thus have lower thermal resistance and provide good heat dissipating paths down to the substrate in vertical direction.

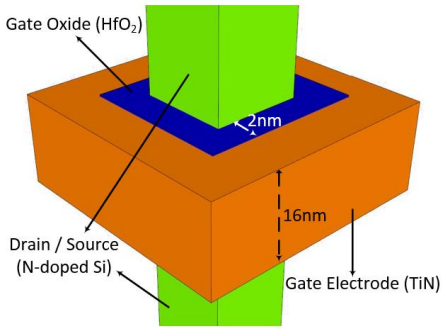

Figure 3. An n-type V-GAA Junctionless transistor in 16-nm S3DC technology.

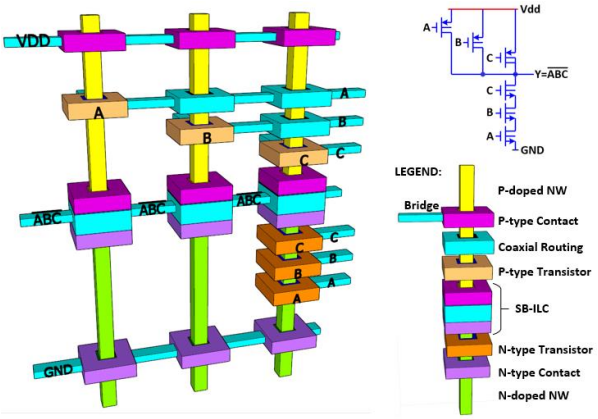

Figure 4. S3DC 3-in NAND gate layout (dielectric for isolation between components and structural support not shown).

HEJs and HEBs can be inserted into standard cell layouts, making the design thermally-optimized. However, HEJs and HEBs lead to connectivity overhead due to the routing resources they are using. Consequently thermally-optimized standard cells are only selectively implemented when the cell temperature is very high, which requires each cell to contain two types of layout designs, with and without thermal features. Any standard cell layout that is not thermally-optimized can still dissipate less of its generated heat through the power rails to HDPPs to substrate, and through vertical nanowires to substrate.

4. S3DC AUTOMATIC THERMAL NETWORK EXTRACTION

The extraction is performed hierarchically in two levels. We are showing the work in the S3DC technology as a case study.

Figure 6 shows an envisioned physical design flow which incorporates a thermal optimization stage. The automatic thermal extraction tool takes the post-placement physical design and the pre-extracted standard cell thermal networks as inputs, and repetitively characterizes the design to serve as the feedback in the thermal optimization loop. In each iteration, the extraction tool generates the thermal resistance network of the design, simulates the network in HSPICE, and measures the results. If the results show that some cells or regions are still too hot, thermal features like HDPPs and thermally-optimized standard cells will be added with probabilistic approach like simulated annealing. The optimization iterates until the whole design is reasonably cool. At last, after the thermal optimization loop, routing is done for signal Bridges as well as HEBs.

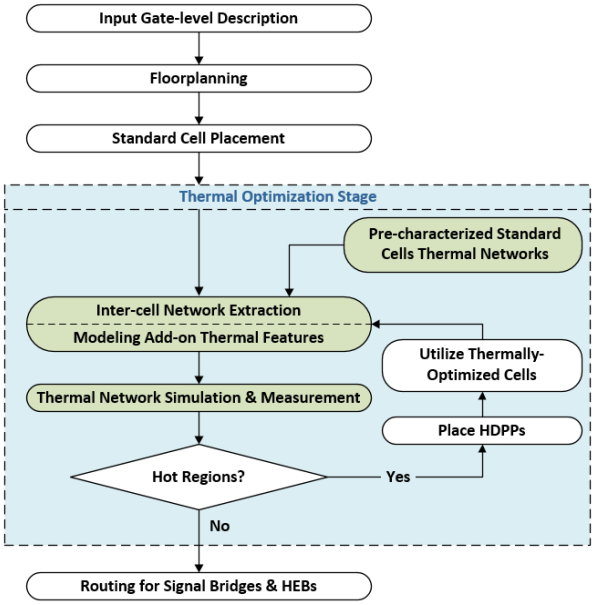

Figure 6. Envisioned physical design flow incorporating thermal optimizations (proposed automatic thermal extraction work shown in green blocks).

Phase 1: Standard Cell Thermal Characterization

The steady-state thermal modeling of standard cells has been done by using the electrical analogue of thermal generation to estimate

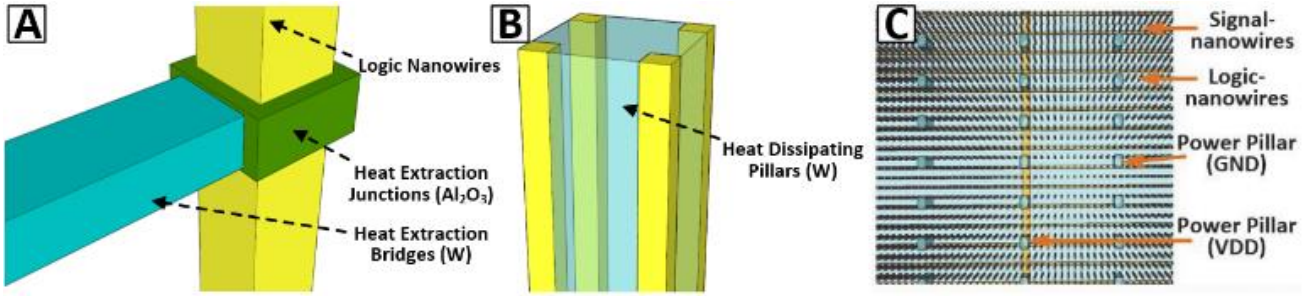

Figure 5. S3DC intrinsic heat management components: A). HDPP; B). HDPPs sparsely distributed in the vertical nanowire template; C). HEB and HEJ connected on a logic nanowire.

temperature gradients [17]. The relationship between heat (Q) and temperature (T) is:

$$\Delta T = R_T * Q = \frac{L}{K * A} * Q$$

where R_T is the thermal resistance of the heat dissipating paths, L is the length of the heat path, K represents the material thermal conductivity, A is the cross-section area of heat path and Q is the heat generated inside a switching transistor. Q and R_T are analogous to current and resistance in electrical domain. By modeling all Q and R_T with current sources and resistors, we can build a thermal modeling circuits with resistors and current sources, and calculate ΔVs using Ohm's Law. ΔV in thermal modeling circuits represents ΔT, the temperature gradient in the layout.

The standard cell layouts have been modeled with thermal resistance networks using this method. All the thermal resistances are calculated based on the material types and the geometries of the structures in the layout; nanoscale effects are captured with calibrated thermal conductivity parameter K values (for example, K is 147 $Wm^{-1}K^{-1}$ in bulk silicon and only 13 $Wm^{-1}K^{-1}$ in thin silicon layer [18], and the effect is considered in our modeling). Generated heat of a switching transistor Q can be calculated by multiplying the drain-source current and the drain-source voltage, I_{DS}*V_{DS}. We consider the worst case when calculating Q: we do transient HSPICE simulations for each cell operation, measure the curves of I_{DS}*V_{DS} and take the peak values during the transition; different operation conditions lead to various results (considering various input patterns, input voltage transition slopes and load capacitances), and we consider the case that leads to the worst result. Figure 7 shows the physical implementation of a thermally-optimized S3DC inverter and its corresponding thermal modeling network as an example.

Phase 2(a): Inter-Cell Network Extraction

After preparing the standard cell thermal models, the thermal network extraction of a S3DC physical design can be done by using the modeled cells and adding the heat paths from inter-cell components, such as power rails, signal wires and thermal features.

First, the automatic thermal modeling network extraction starts with a post-placement physical design of an S3DC circuit. The input file is in DEF format and generated by SoC Encounter. The thermal extraction tool reads the DEF file, and acquires the information on cell placement, dummy filler insertion and the terminals that need to be connected. With the cell positions and the built thermal models of each cell, we can build an initial thermal modeling resistance network.

Then the heat paths from power rails are added into the resistance network. In S3DC, we are assuming that mesh structures are used for power delivery. The power mesh connects a nanowire to all its four neighboring nanowires with power Bridges, and connects to the power sources on chip. We model its effect on thermal features by adding a heat path in between each pair of adjacent nanowires at the top and the bottom of the nanowires.

An inter-cell signal connection can be also modeled as a heat path between cells that are connected by the signal wire. For a two-terminal net case, the thermal resistivity of the heat path is estimated based on the Manhattan distance between the two terminals. A multi-terminal net can be converted into a set of two-terminal nets and then modeled. The conversion can be done with the Minimum Spanning Tree method for good efficiency; we have used Prim's algorithm to find the Minimum Spanning Tree representing each multi-terminal net. A clock signal can be treated as a multi-terminal net that connects to all sequential elements.

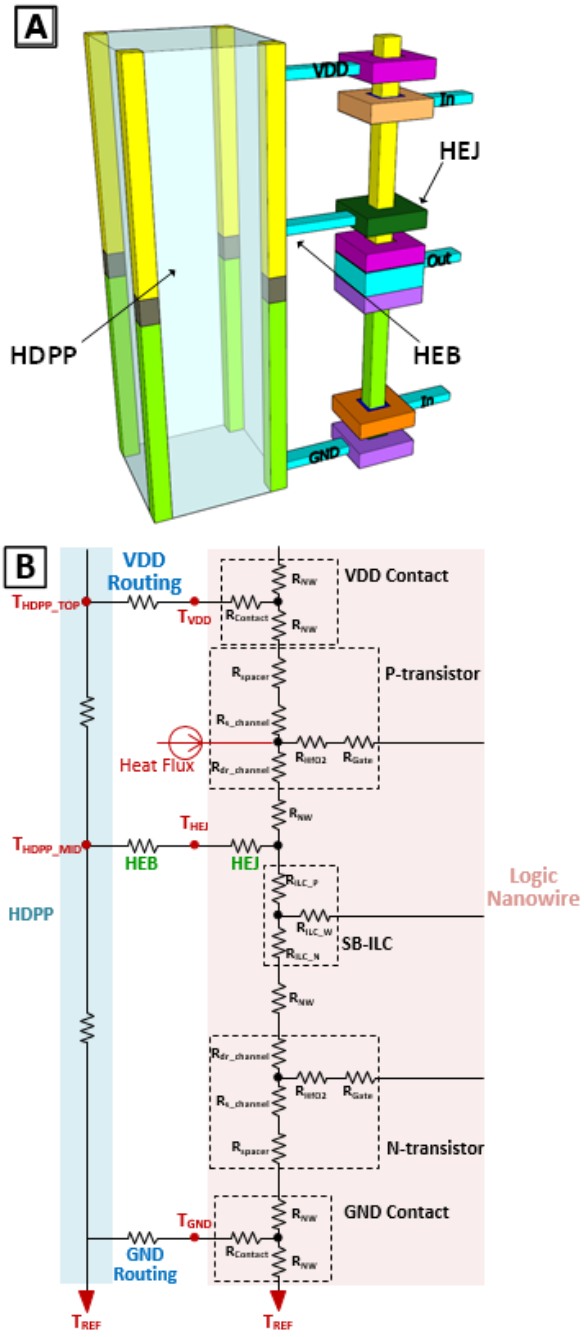

Figure 7. A). thermally-optimized layout of S3DC inverter; B). thermal modeling network showing the case during p-type transistor switching.

Phase 2(b): Modeling Add-on Thermal Features

At last, the resistances modeling the added HDPPs, HEJs and HEBs are added into the thermal resistance network. HDPP is connected to power delivery mesh and adds additional heat dissipating paths down to the substrate, so it is modeled as a thermal path with one end connected to the substrate and the other connected to nearest power delivering wires. HEJ & HEB in the thermally-optimized standard cell layouts add lateral thermal paths to HDPPs, so it is modeled as a thermal path connecting the cell to its nearest HDPP.

After extracting the thermal modeling resistance network for the input physical design, HSPICE simulates the extracted network, calculates and measures all the node voltages, which represent the temperatures in the input physical design.

5. THERMAL CHARACTERIZATION RESULTS

In this section, several benchmark circuits have been evaluated using the proposed methodology and the results of thermal characterization are shown by including thermal maps. We also show comparisons between circuits with and without implementing thermal management features. The results indicate that our method captures the effect of thermal management features at fine granularity to drive circuit-level thermal mitigation with thermal features included. Until experimental validation becomes available such fine-grained thermal characterization could also act as a reference for creating higher-level thermal models that could further reduce thermal evaluation complexity – especially when used as part of a 3D CAD flow.

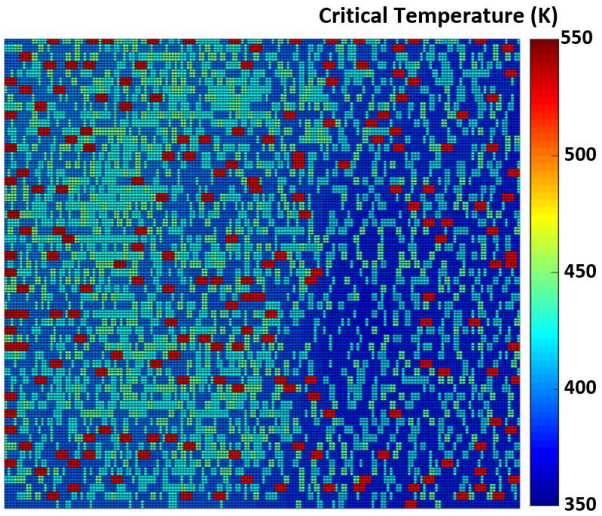

Figure 8. 16-bit multiplier (C6288 ICSAS benchmark) thermal map (top-down view).

During HSPICE simulations of extracted thermal modeling networks, the worst-case hot spot temperatures in all cells are measured (MATLAB is then used to plot the measured results and generate the thermal maps included in the paper). The physical design we have used as the input is a 16x16 multiplier (ISCAS C6288 benchmark) after the placement stage, which is generated following the Skybridge semi-custom design flow shown in [19]. Figure 8 shows the thermal map of the design without any thermal features. As we can see, many cells are with very high temperatures. From the thermal maps, it is easy to target the thermally critical cells and then optimize them during the later design stages. This piece will be automated in our future CAD flow to synthesize 3D circuits with thermal mitigation features.

We have also done comparisons between the designs with and without implementing the thermal features. Based on the previously shown 16x16 multiplier design, we added an HDPP in the design, repeated the thermal modeling extraction, simulation and measurement, and did the comparison. Figure 9 (A) plots the temperature difference, showing larger temperature reduction in the cells nearer to the HDPP, which is the same as we have expected since the cells nearer to the HDPP have shorter heat paths to them.

We have also implemented one thermally-optimized standard cell with the HEJ & HEB connected to its nearest HDPP, showing a more than 100K temperature reduction in the thermally-optimized cell as shown in Figure 9 (B).

Totally three benchmarks have been implemented in S3DC technology and thermally characterized. Processing the input DEF file and extracting thermal resistance network took negligible runtime, and the simulation times of extracted thermal resistance networks are shown in Table I. Further optimizations on runtime with simplified model can be done when the proposed method is used in thermal optimization, which needs to repetitively do the thermal characterization.

Table 1. Simulation times of extracted thermal modeling resistance networks per iteration

Benchmark	Cell count	Simulation Time (s)
8-bit multiplier	541	1.88
16-bit multiplier	2484	8.41
S13207	8603	34.6

6. CONCLUSION

The article proposes a methodology of automatically extracting the steady-state thermal resistance network from a post-placement physical design, and using HSPICE simulation for thermal characterization. The method first does the fine-grained thermal modeling for the standard cells, and then considers detailed inter-

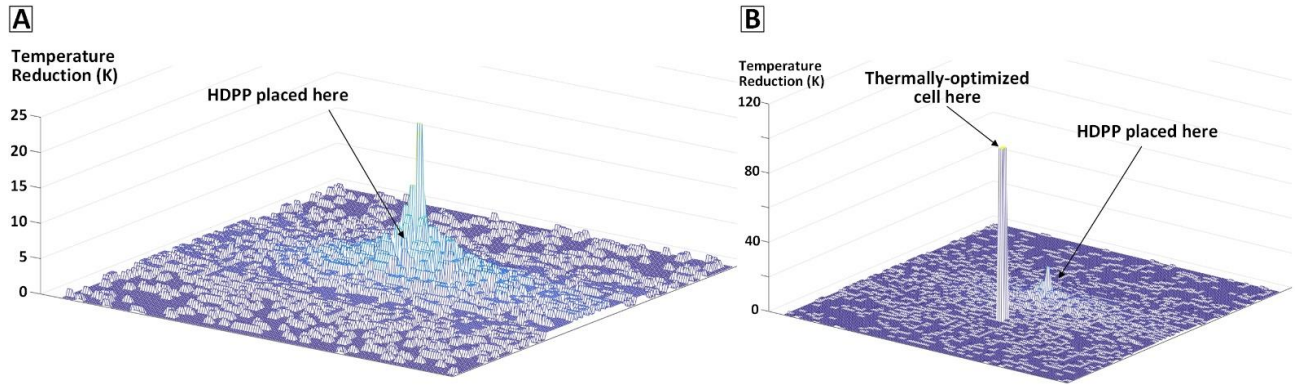

Figure 9. Temperature reduction between design with and without thermal features: A). temperature reduction after one HDPP is placed; B). temperature reduction after one HDPP and one thermally-optimized cell are implemented.

cell routing information as well as the effects of intrinsic fabric-level thermal management features. The method has been utilized in the case of Skybridge-3D-CMOS technology. Potential future directions can be improving the runtime of thermal modeling network simulations with methods such as model order reduction, and developing thermal optimization methods and tools. In particular, methodologies can be developed based on the proposed work to automatically include thermal management components into circuits.

7. ACKNOWLEDGMENTS

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